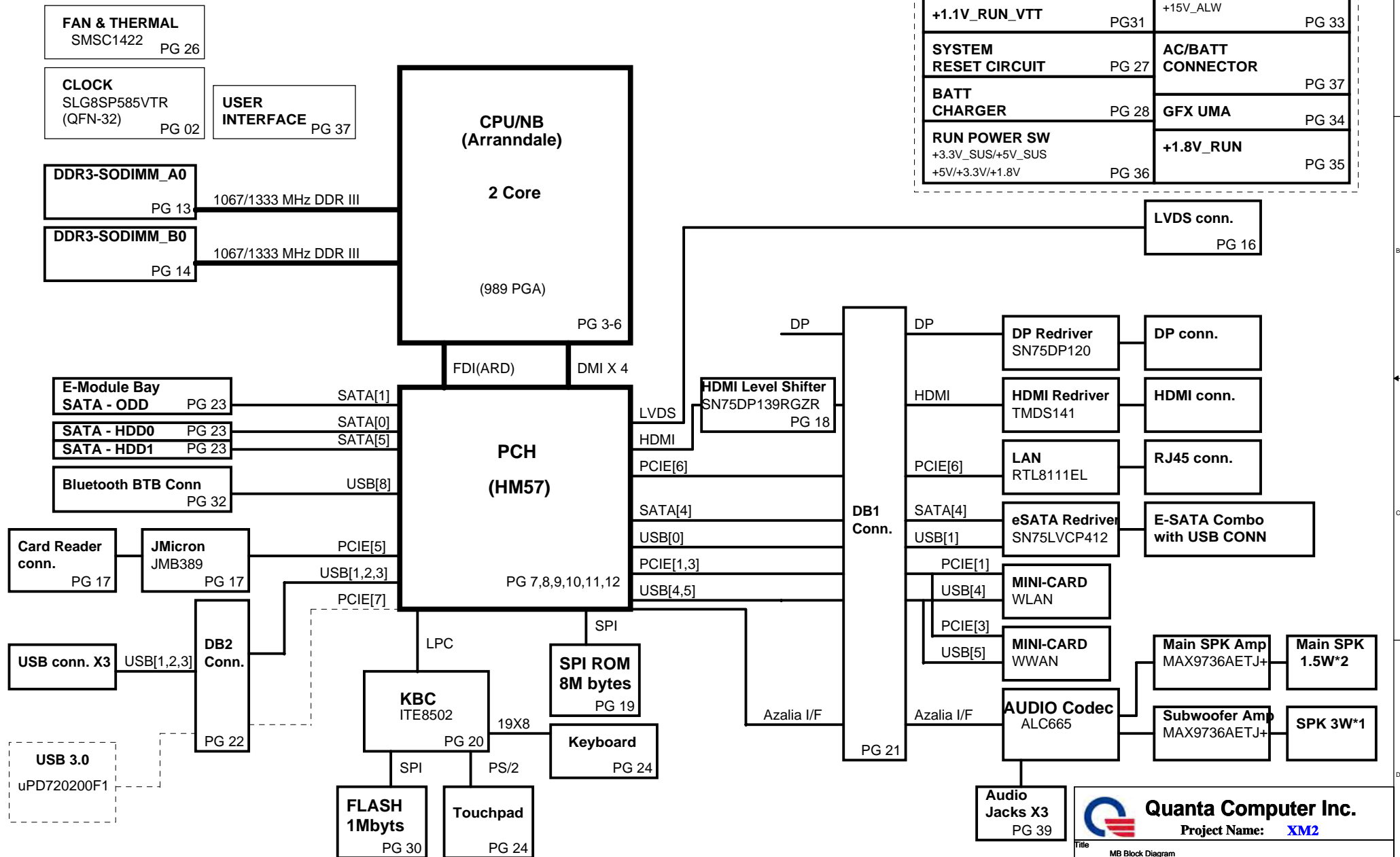
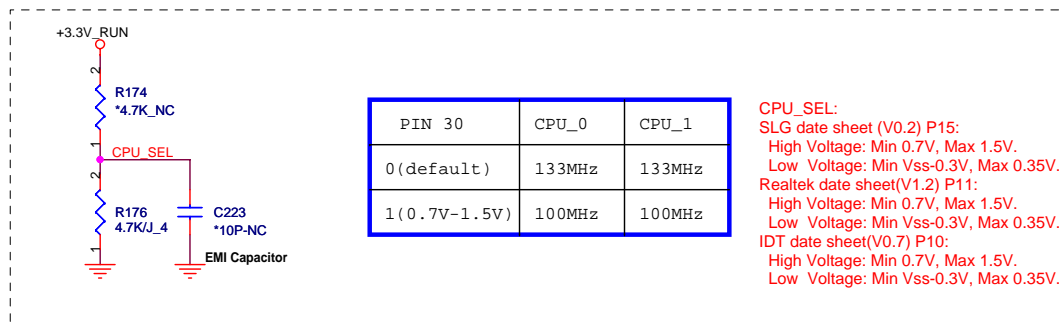
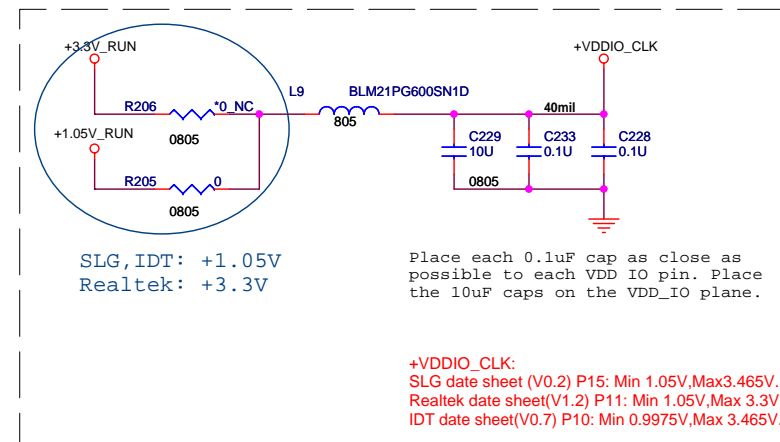
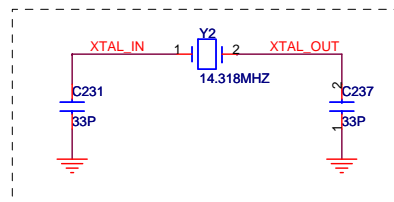
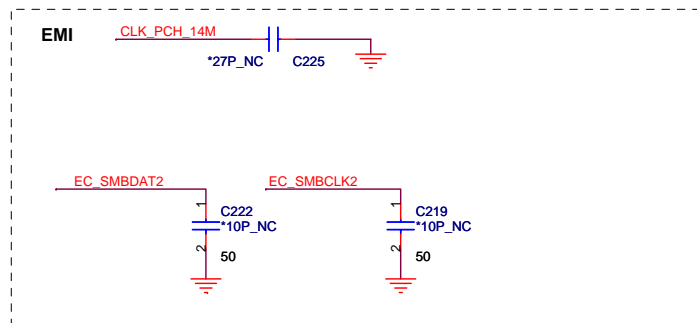
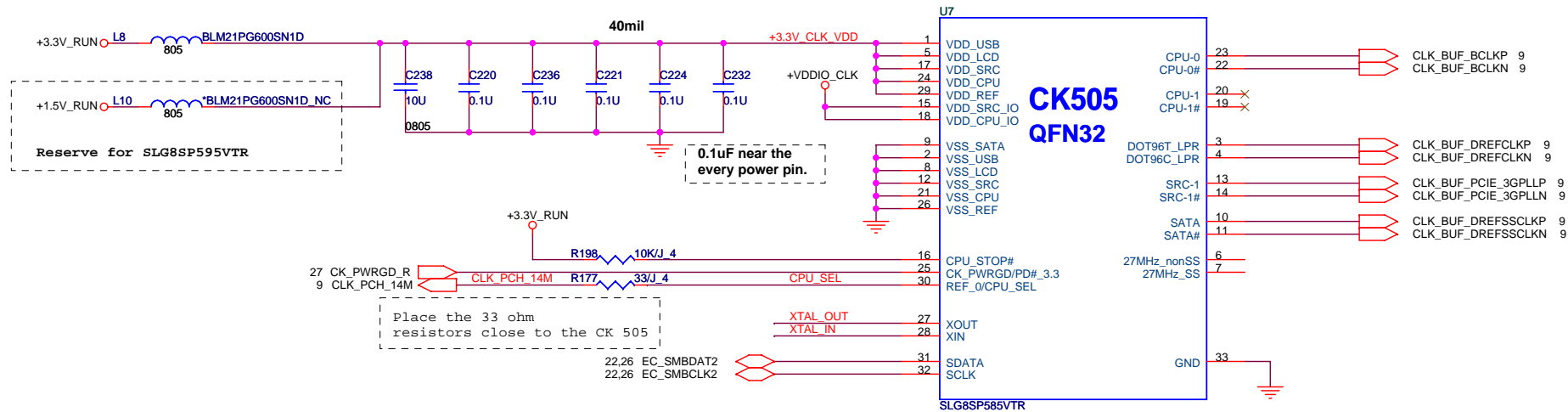
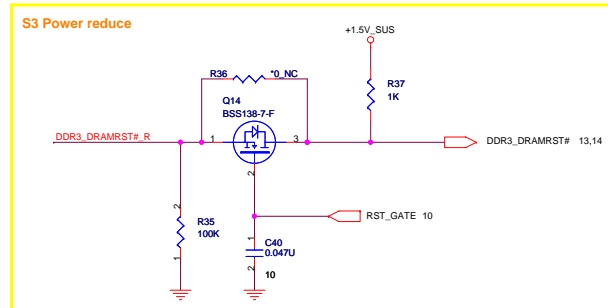
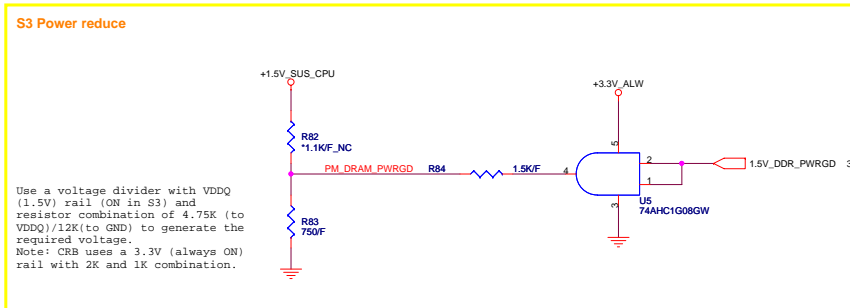
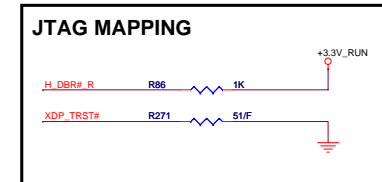
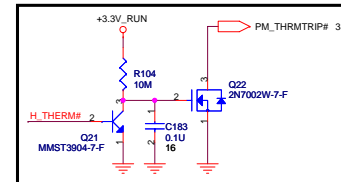
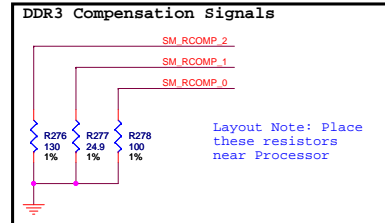
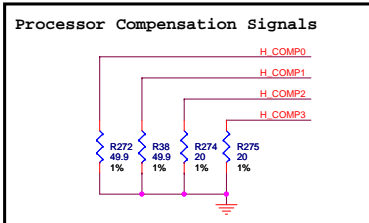
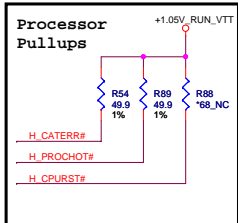
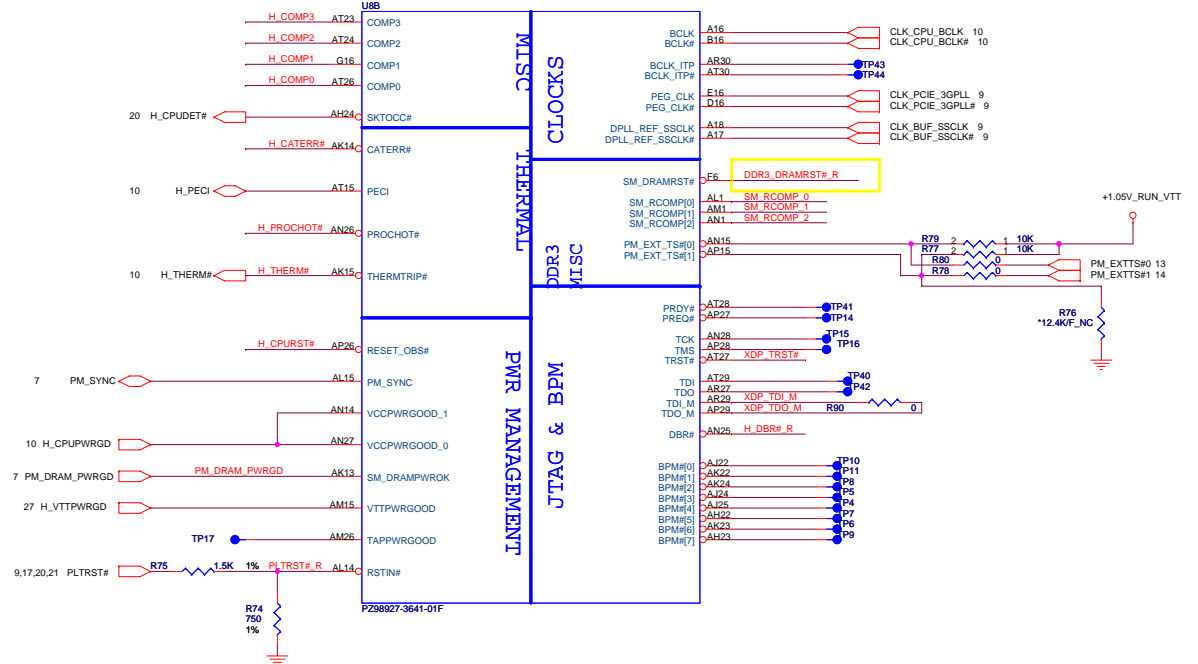
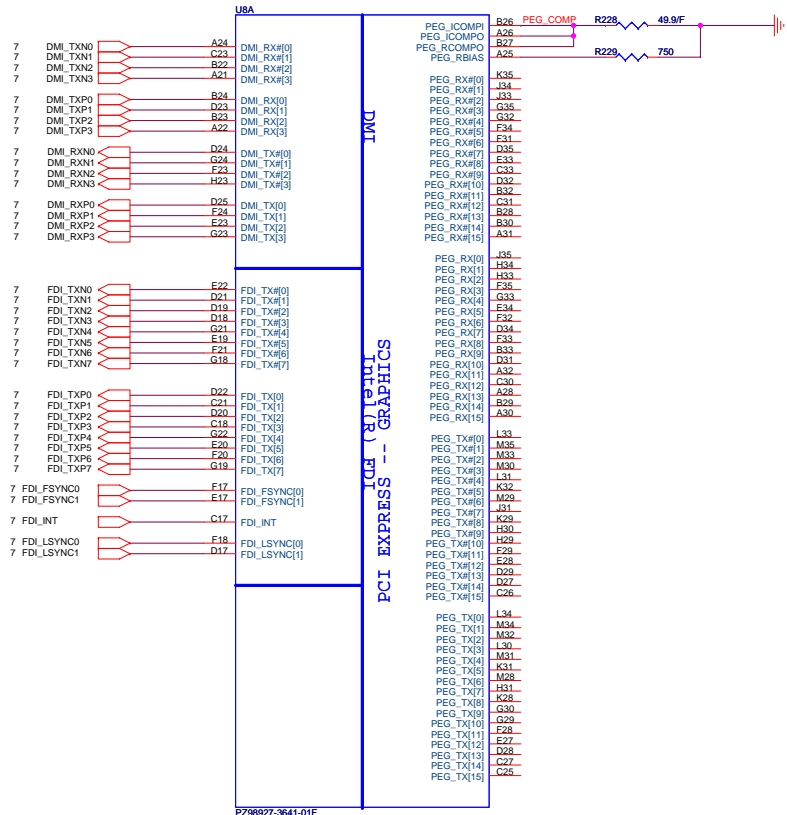
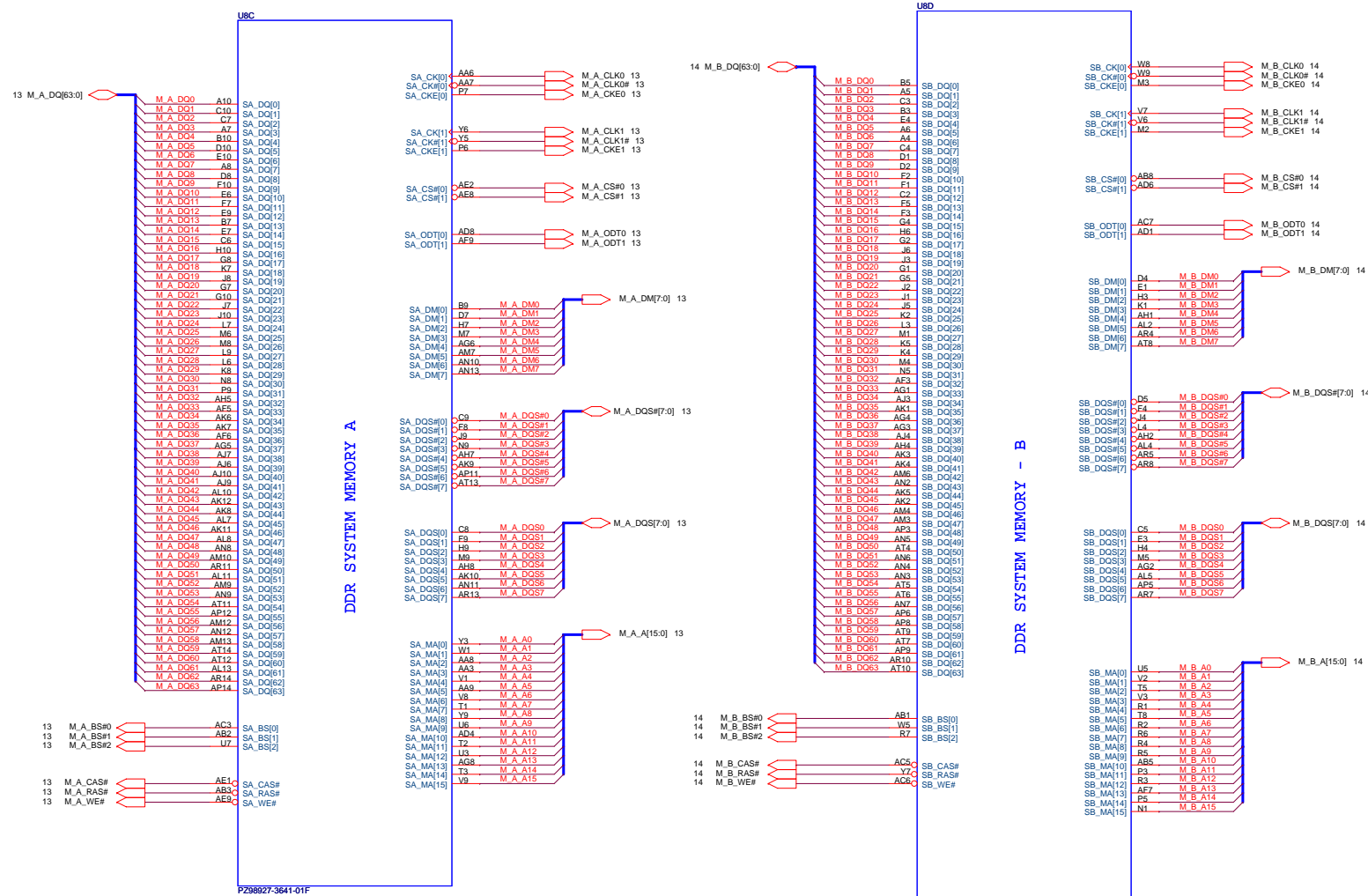


System Block Diagram of GM7









P298927-3641-01F

P298927-3641-01F

**Quanta Computer Inc.**Project Name: **XM2**

Title

CPU 24(DDR)

Size

Document Number

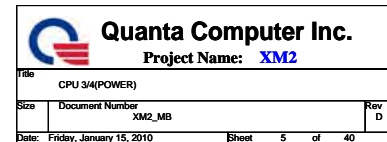
XM2_MB

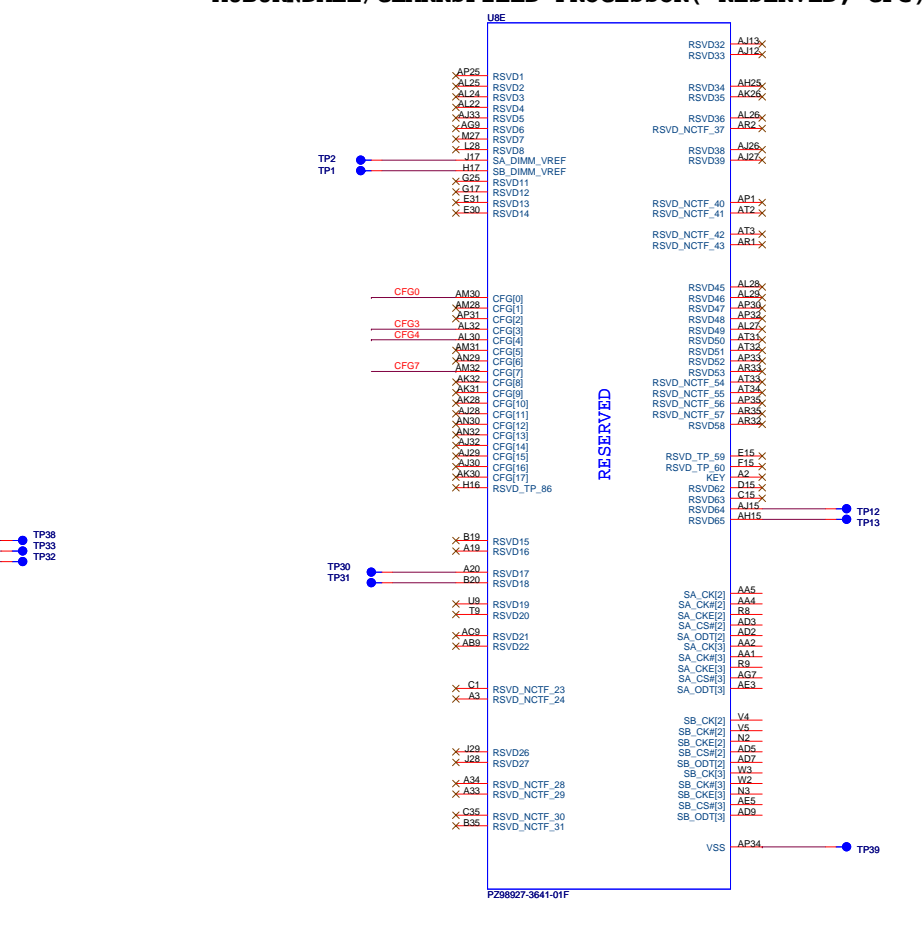
Rev

D

Date: Friday, January 15, 2010

Sheet 4 of 40

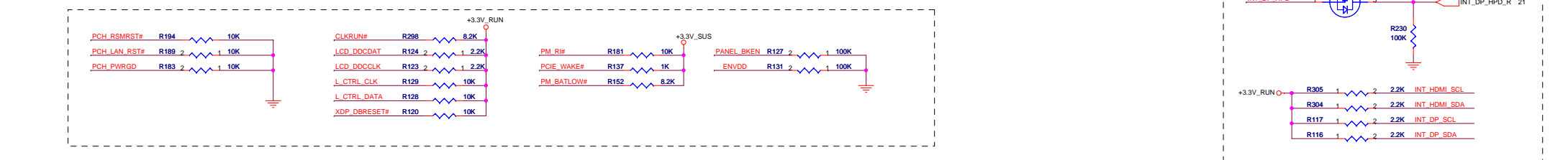
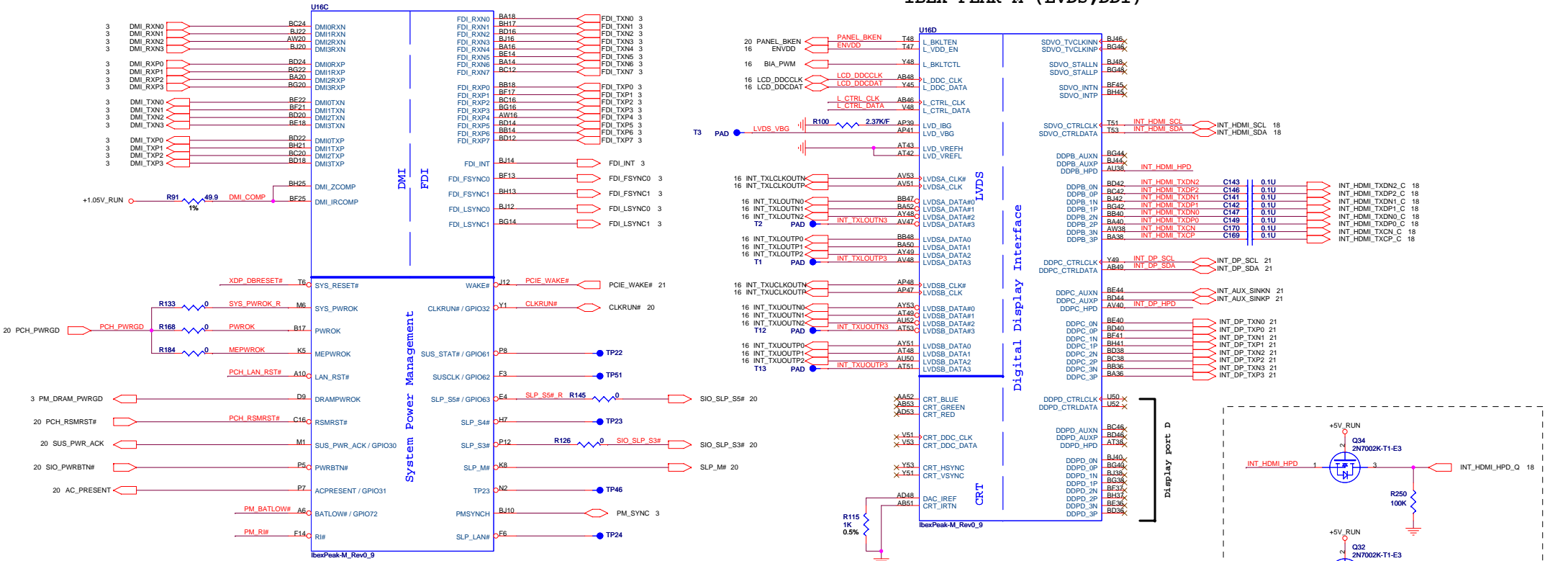


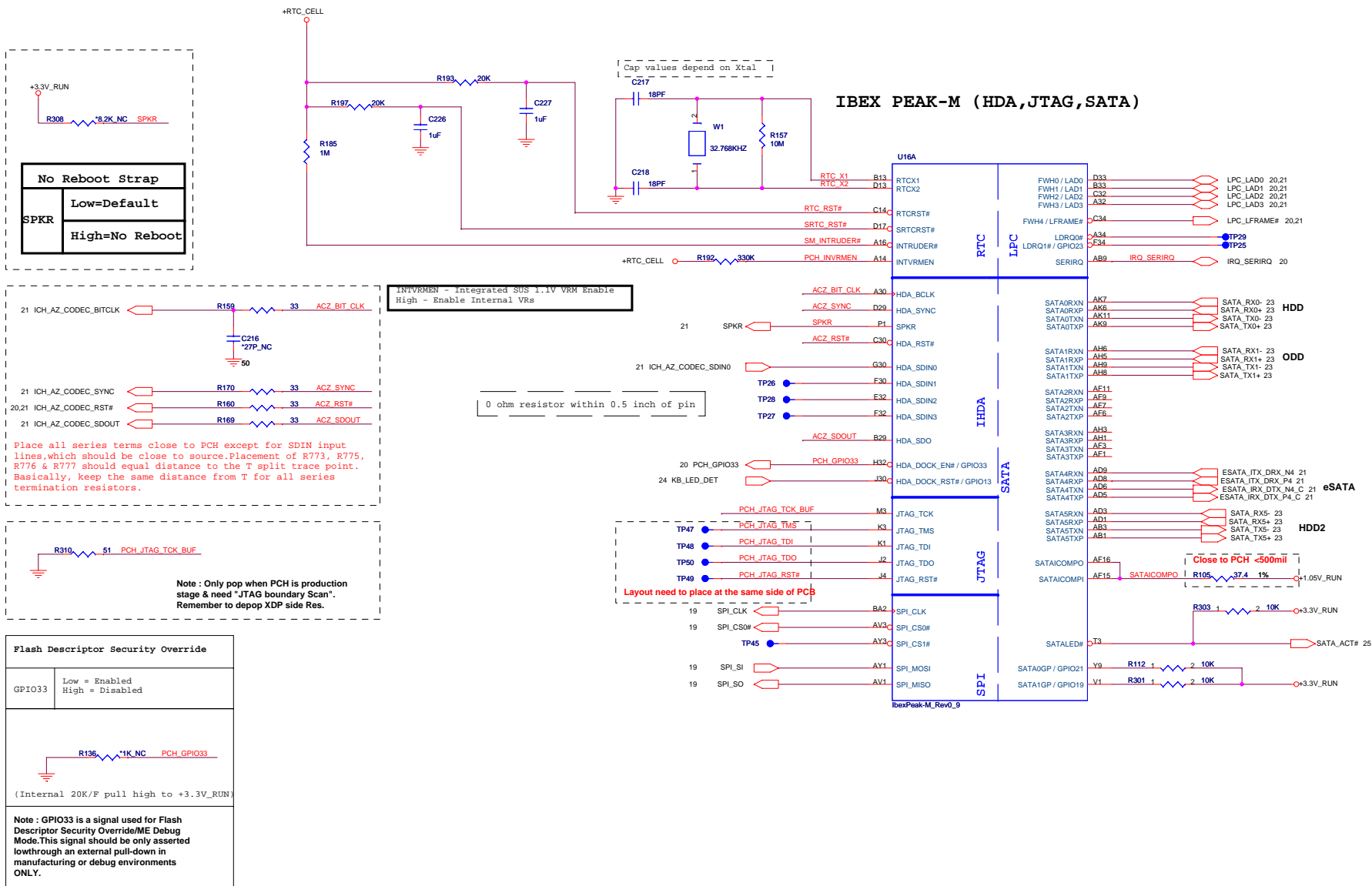


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarksville (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD

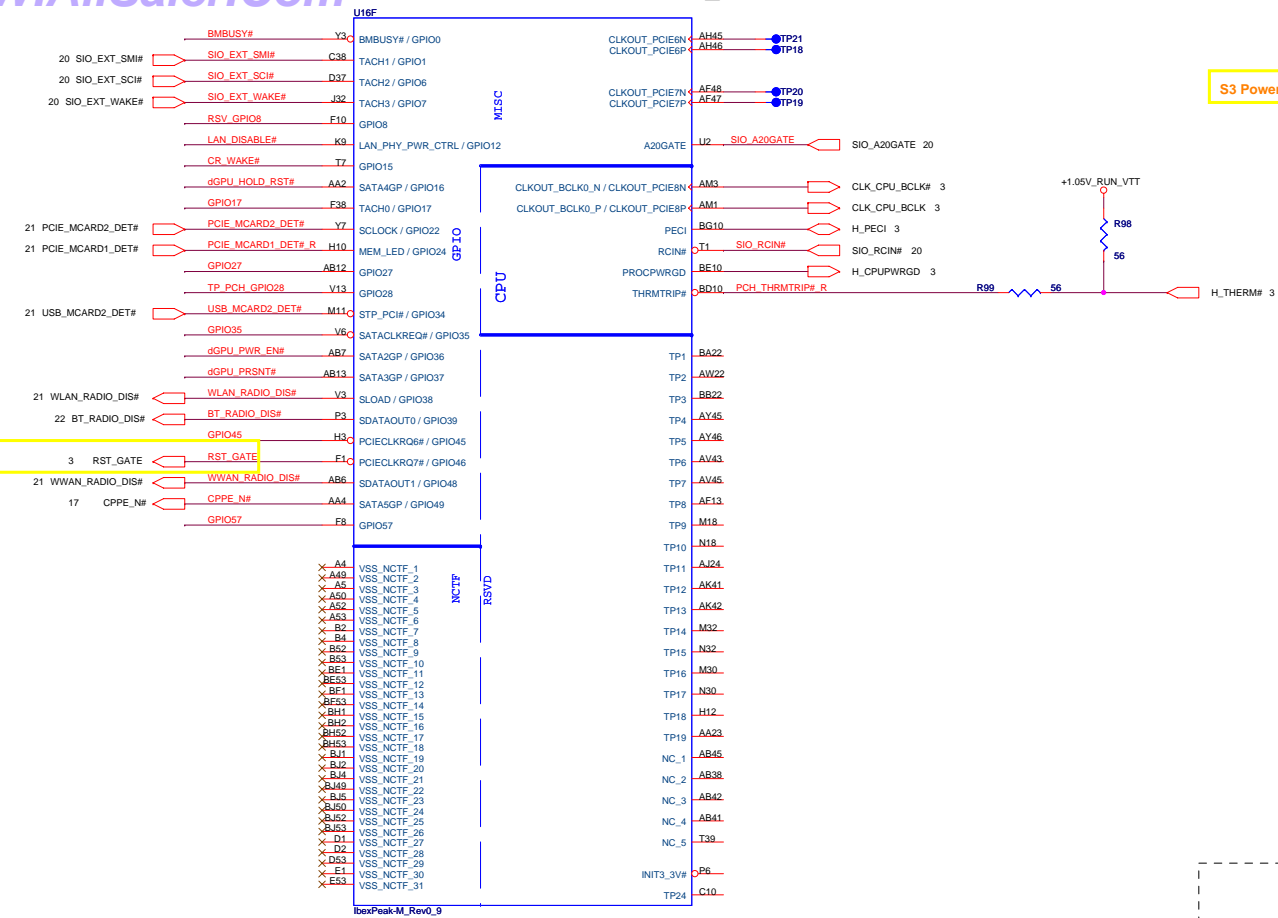
IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (LVDS,DDI)



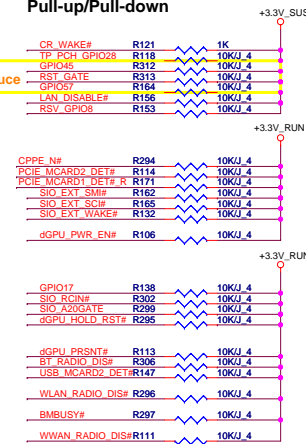


IbexPeak-M_Rev0_9IbexPeak-M_Rev0_9

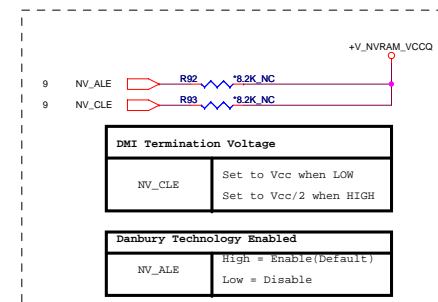
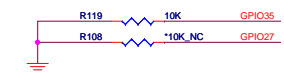
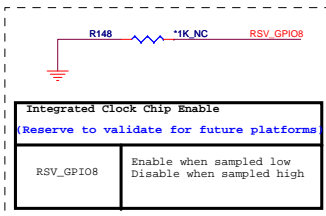


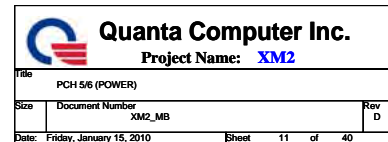
GPIO

Pull-up/Pull-down

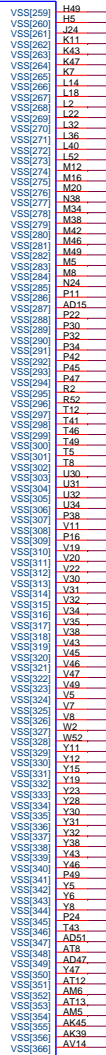
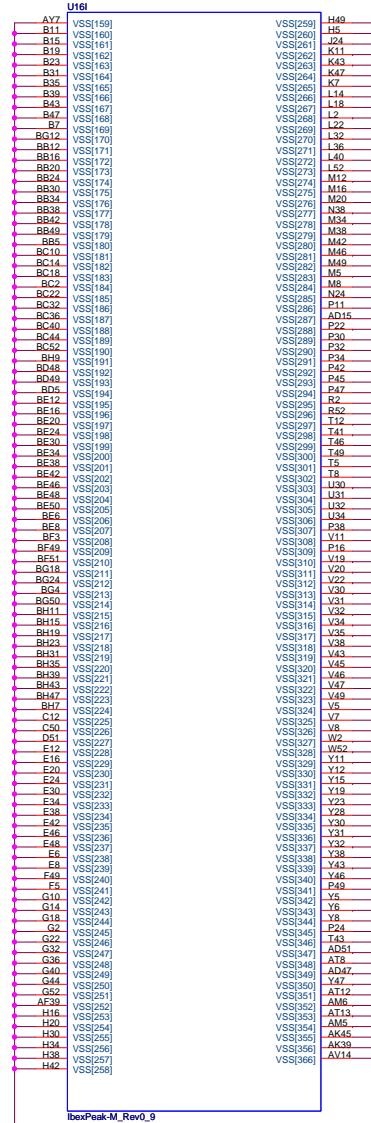
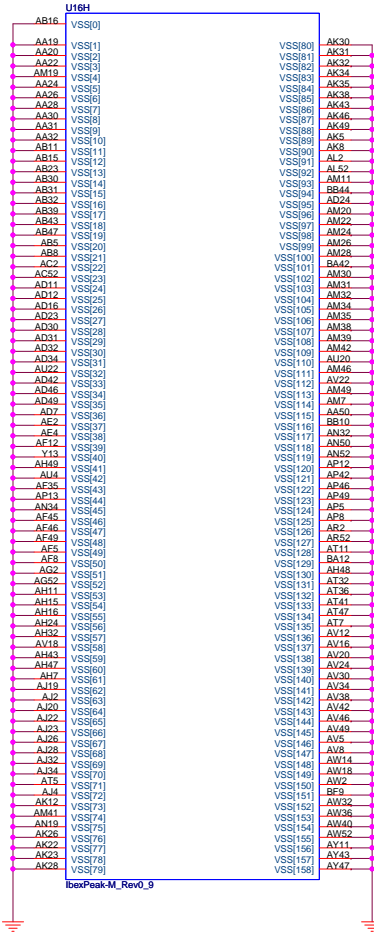


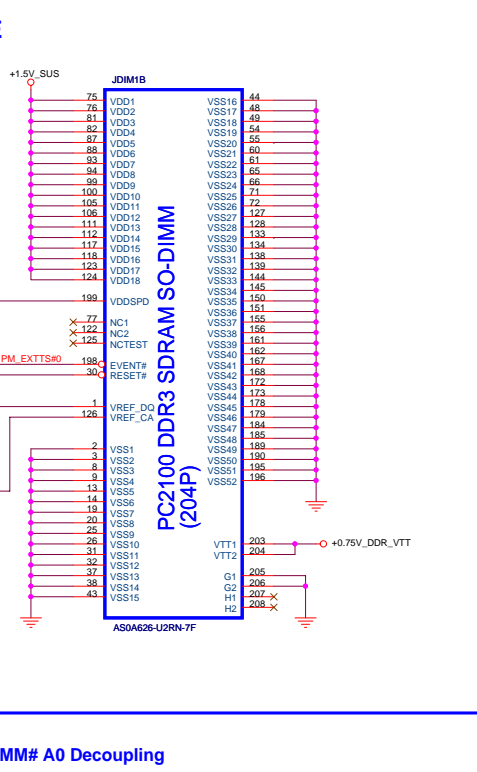
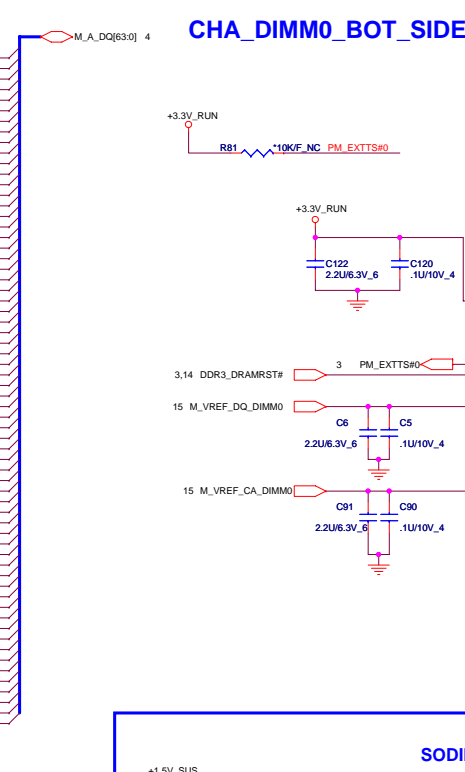
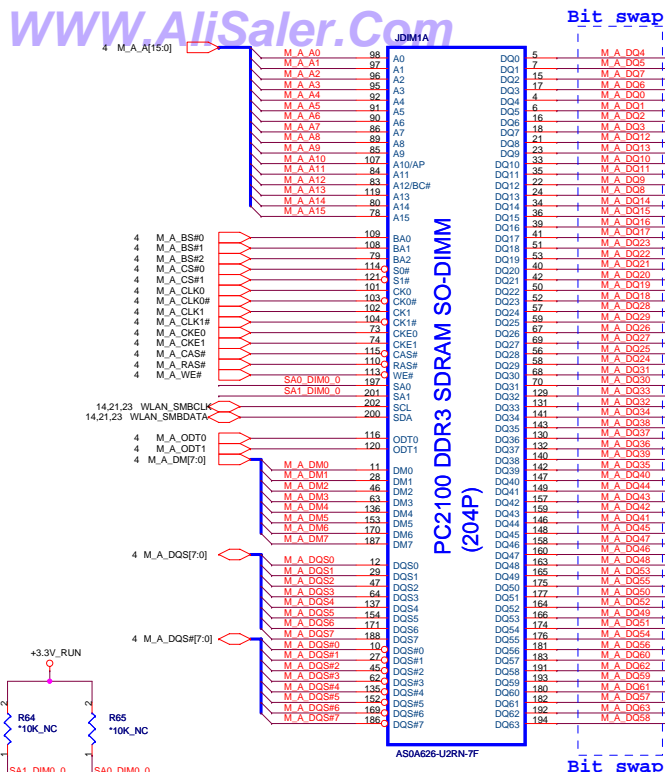
SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------





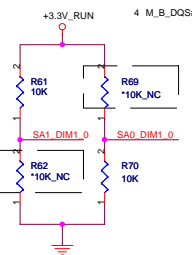
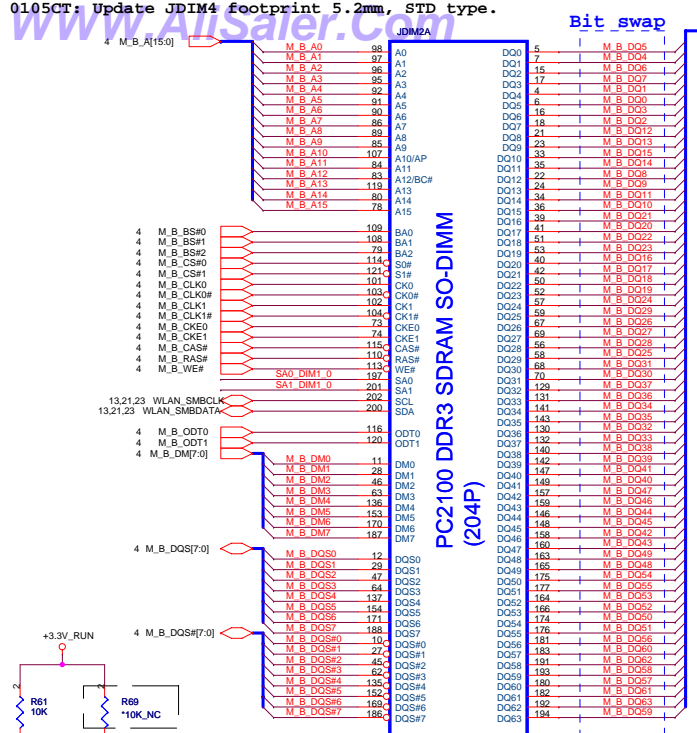
IBEX PEAK-M (GND)





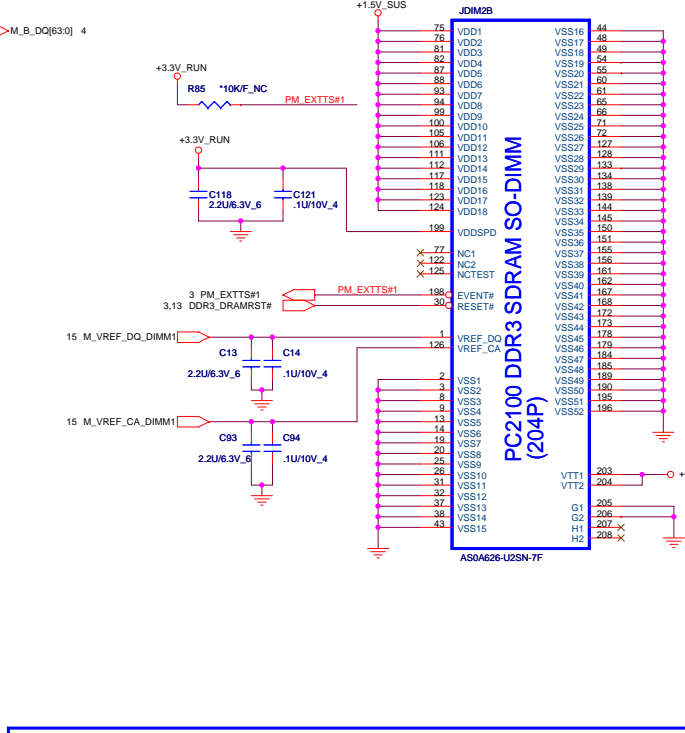
0105CT: Update JDIMM4 footprint 5.2mm, STD type.

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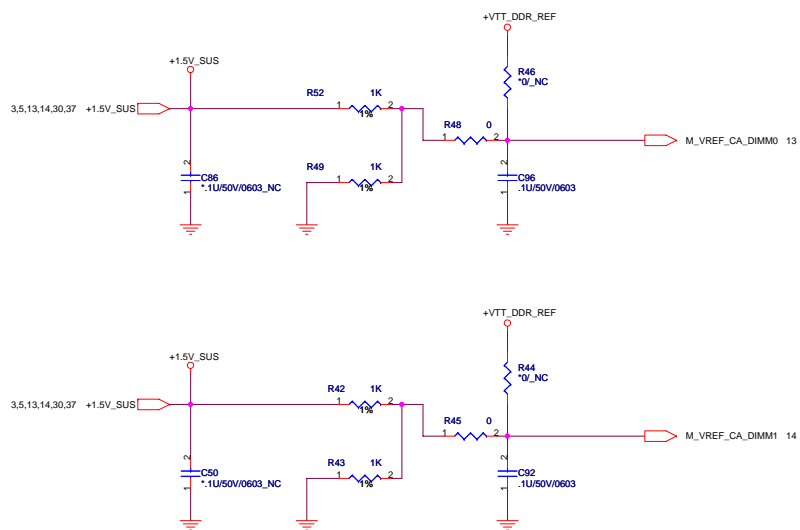
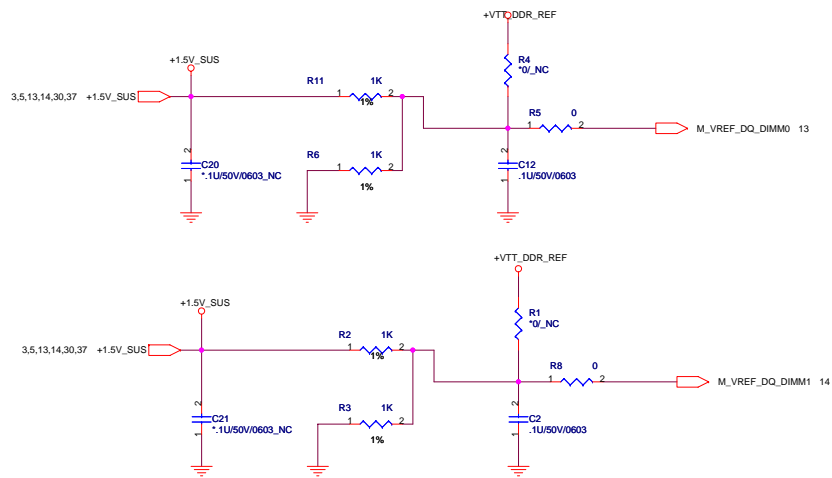


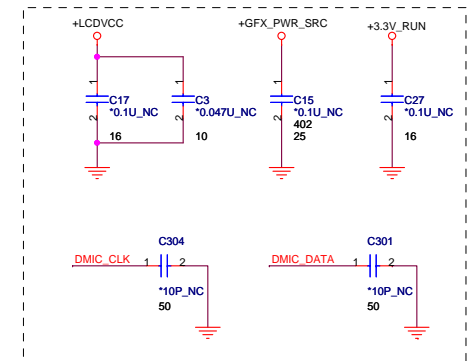
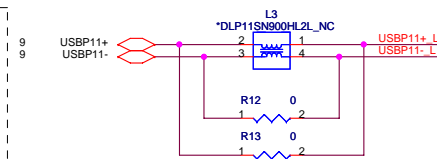
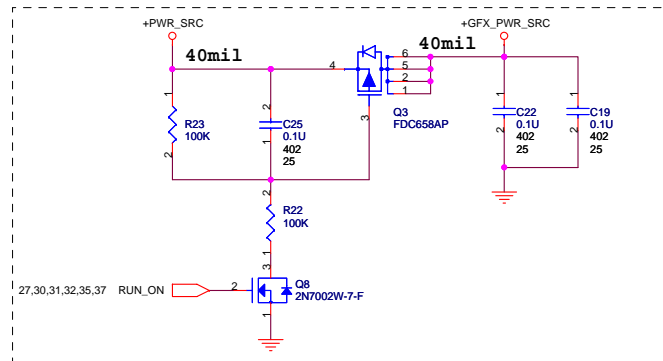
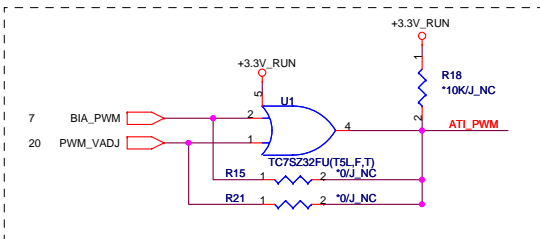
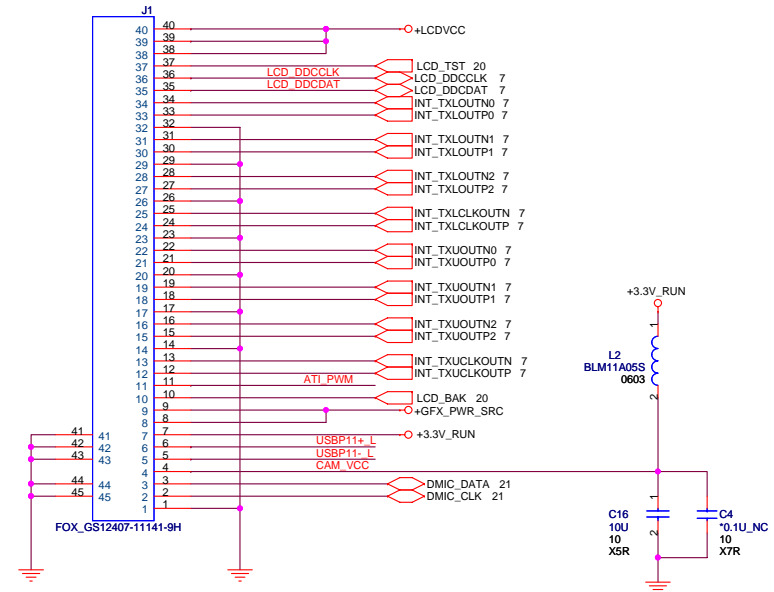
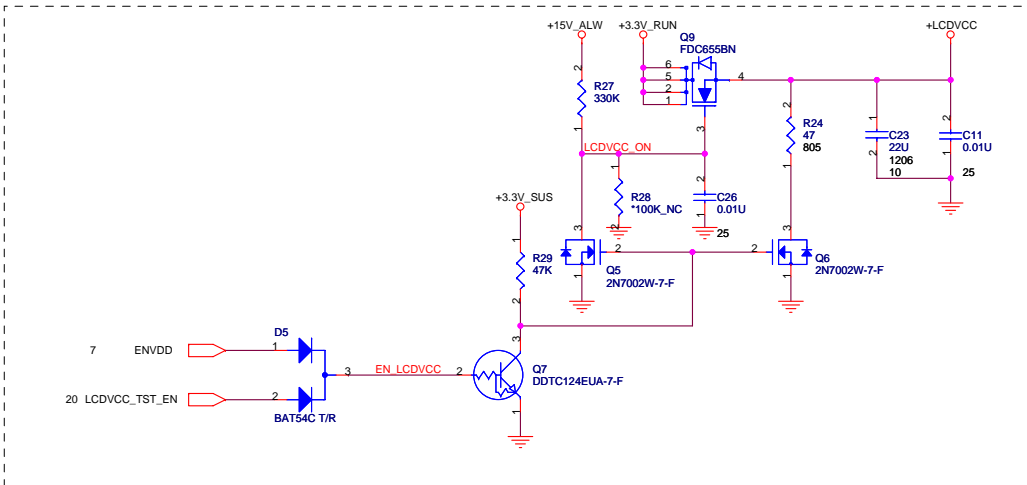
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



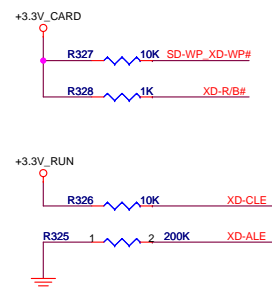
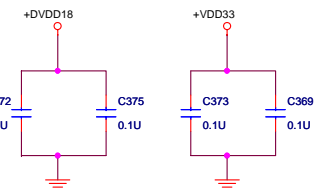
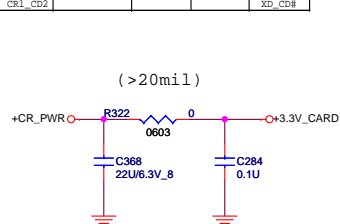
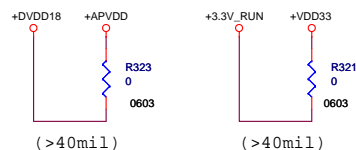
Fixed SO-DIMM VREF_DQ (M1): Default



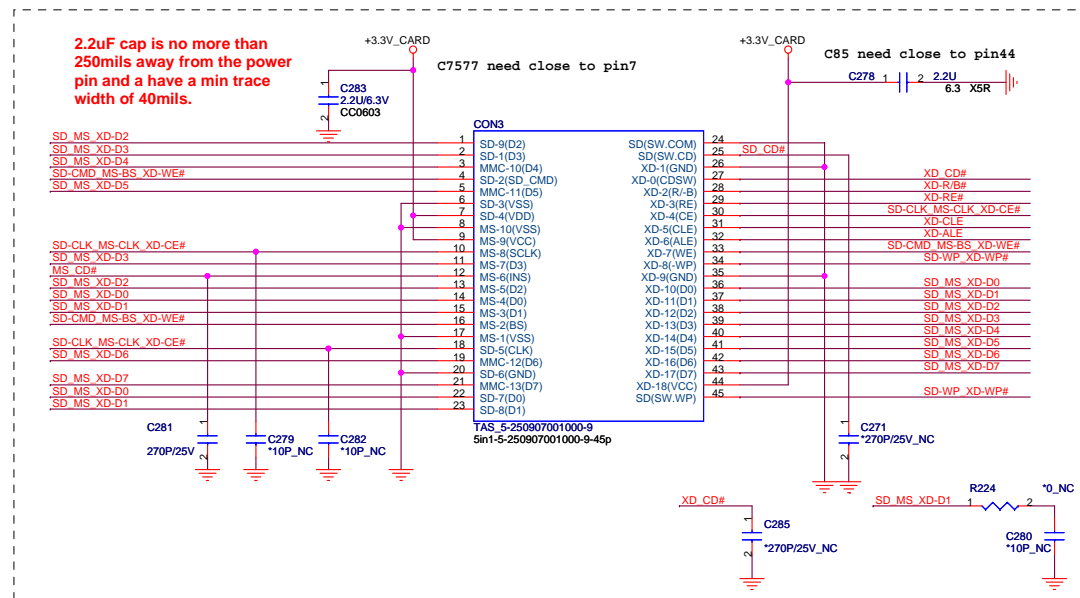
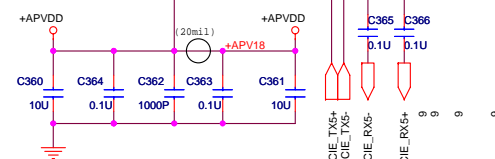
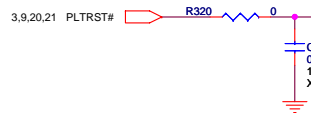


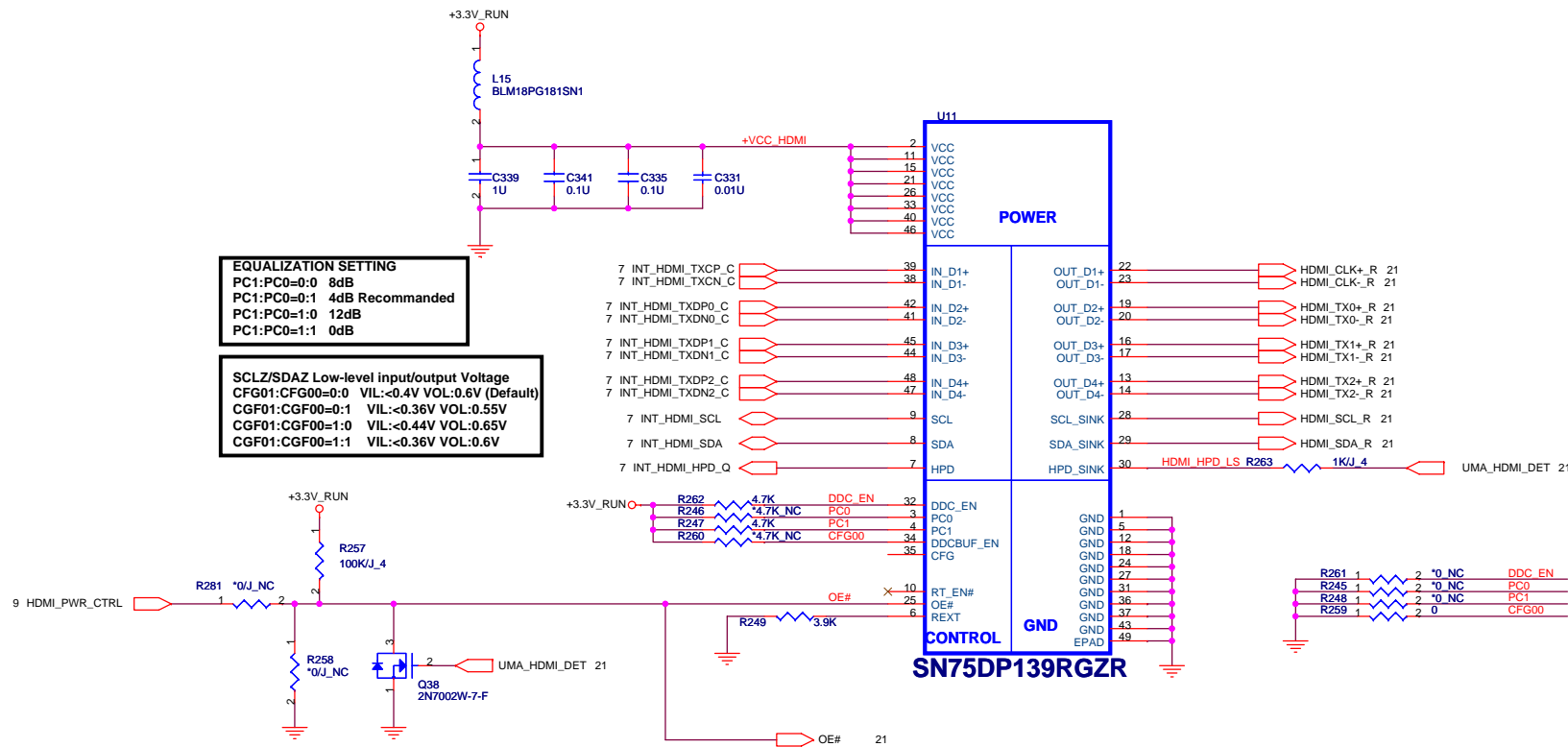
Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/XD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD2			MS_CD#	XD_CD#

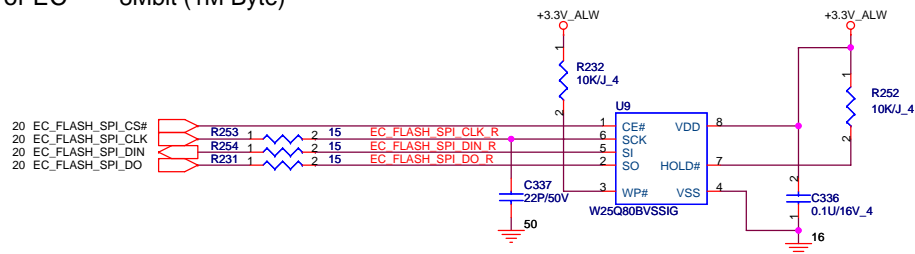


MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3 Application

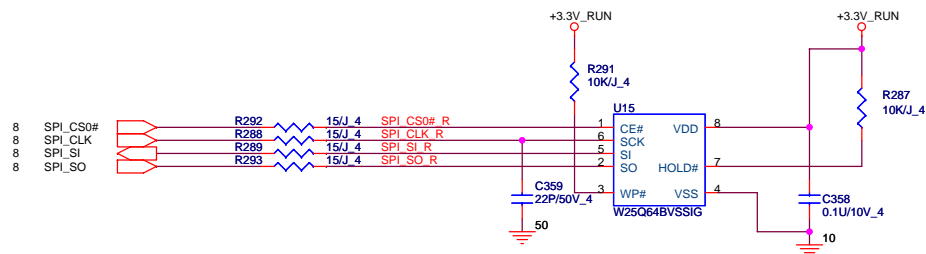




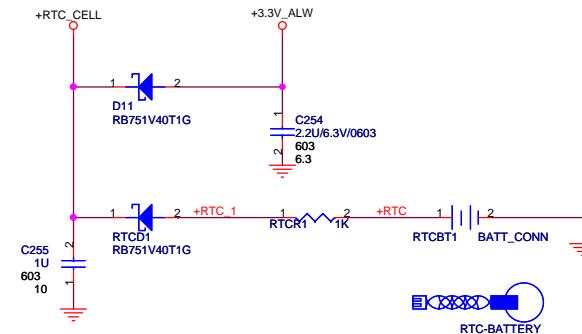
For EC 8Mbit (1M Byte)



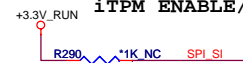
For PCH 64Mbit (8M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE



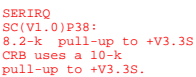
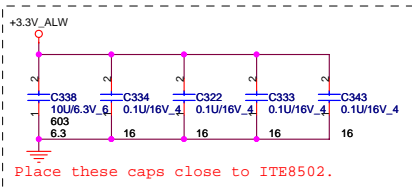
TPM Function	R712
Enable	Mount
Disable	NC (Default)



Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
FLASH / RTC	19	1A

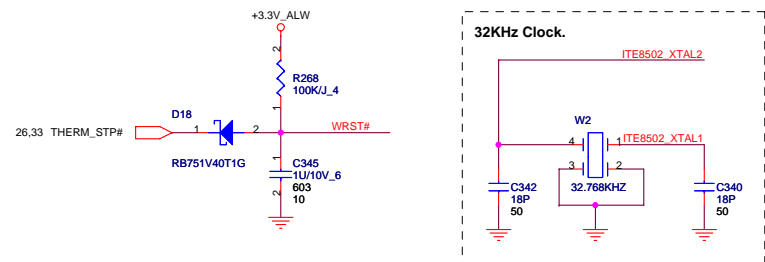
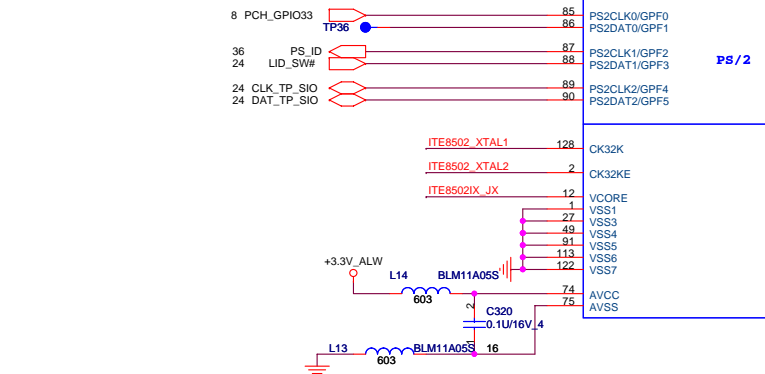
Date: Friday, January 15, 2010 Sheet 19 of 40



Charge and BAT

PCH

MMB, CLOCK, THERMAL



KEYBOARD

ADC/DAC

PWM

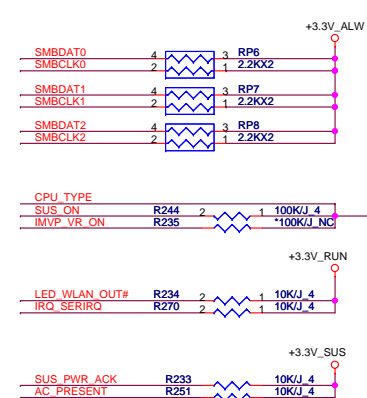
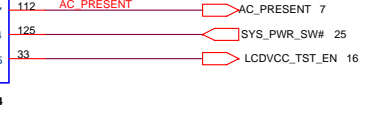
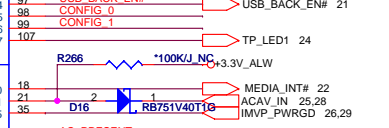
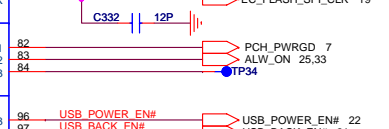
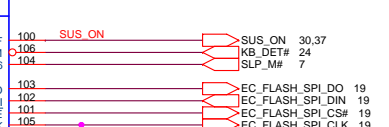
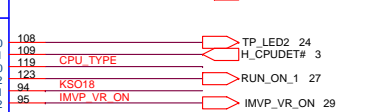
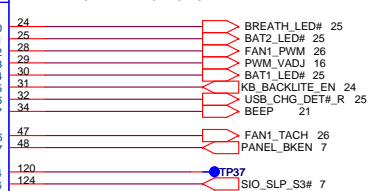
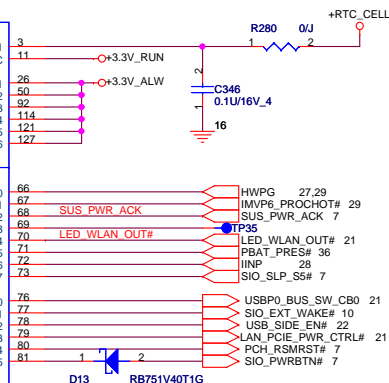
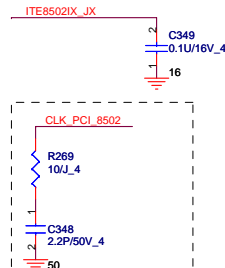
IR/UART

LPC/FWH

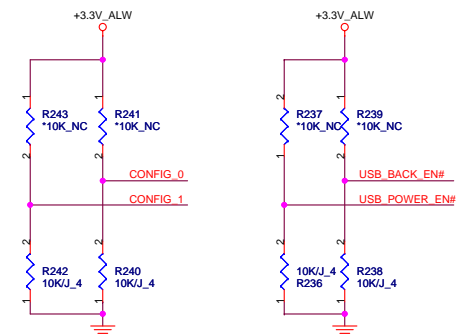
100

EGBC

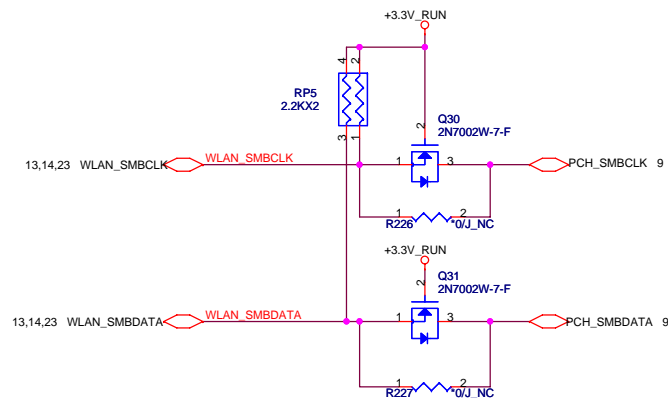
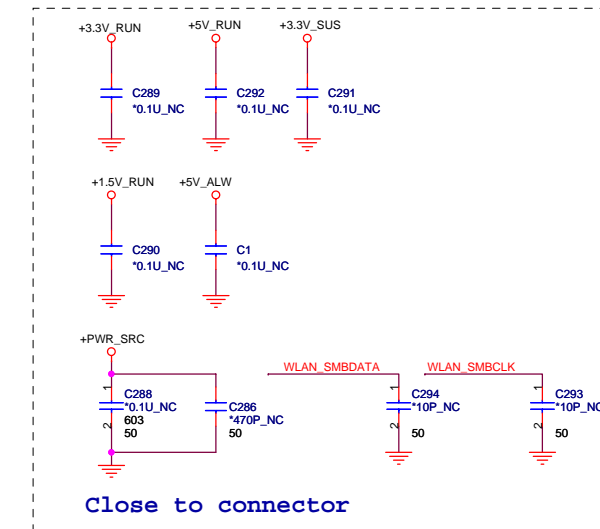
GPIO



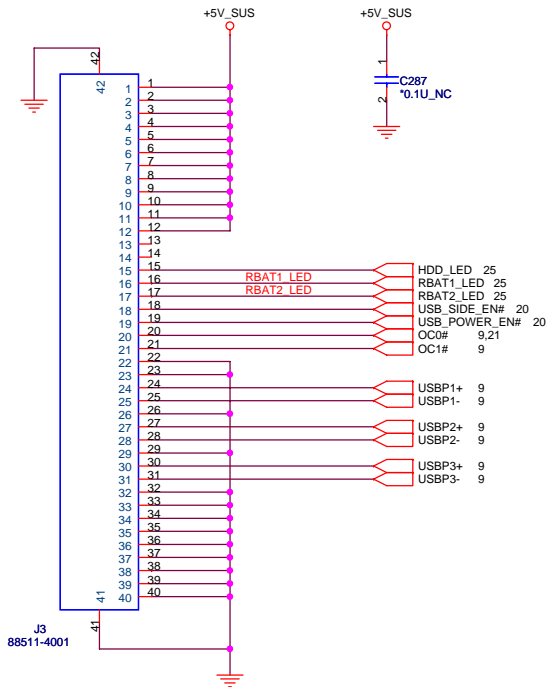
Board ID Straps



Config_0	Config_1	GM7/GM7B
0	0	UMA
0	1	Studio Switchable
1	0	Studio Discrete

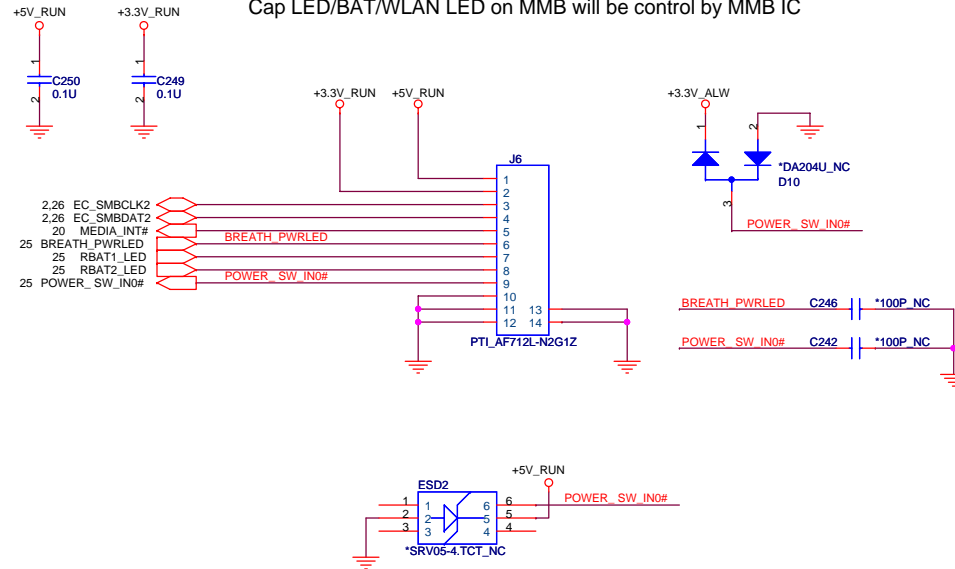


USB IO 40 pins

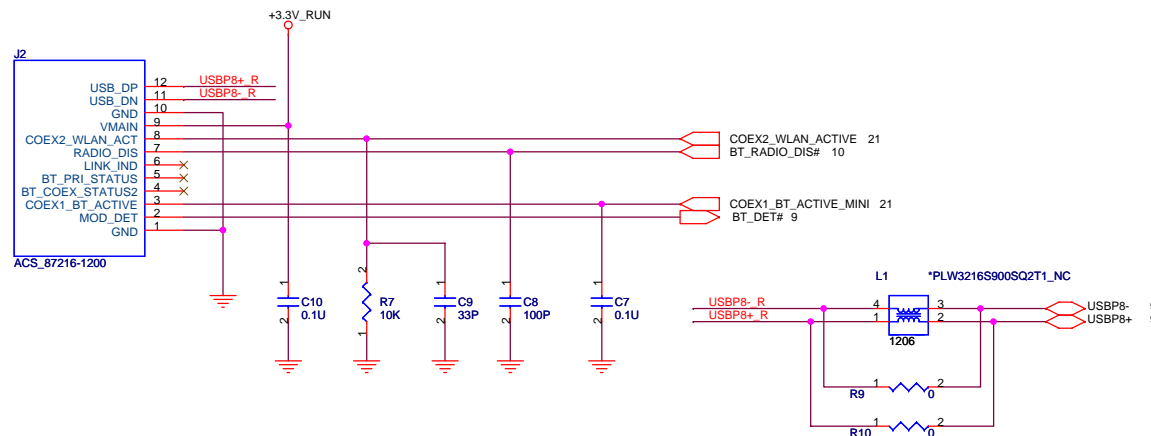


MMB & Power Board 12pins

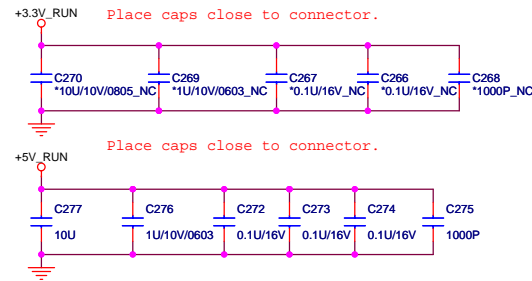
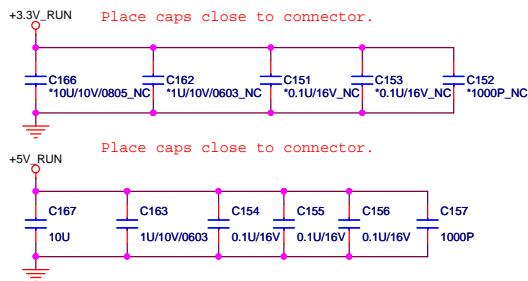
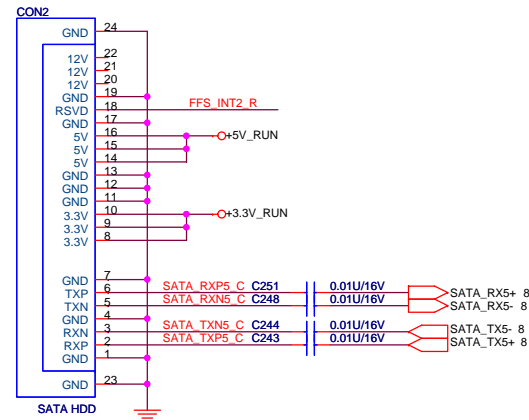
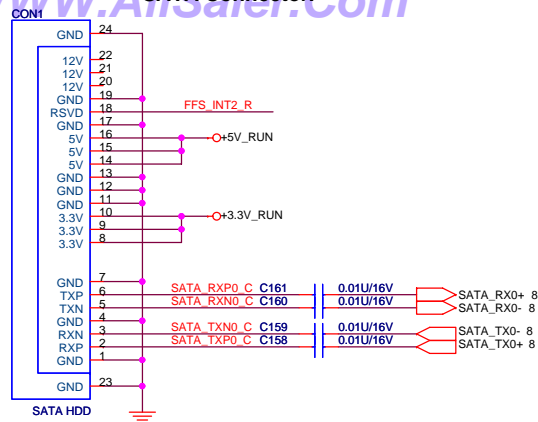
Cap LED/BAT/WLAN LED on MMB will be control by MMB IC



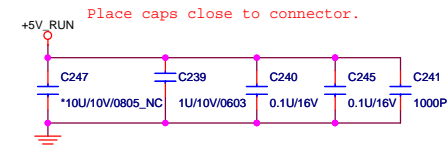
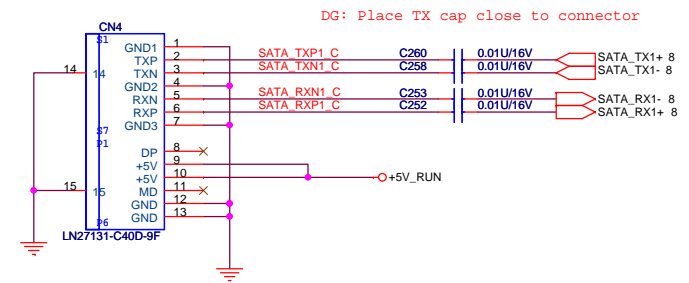
Support Dell BT3xx series module Bluetooth WTB Conn



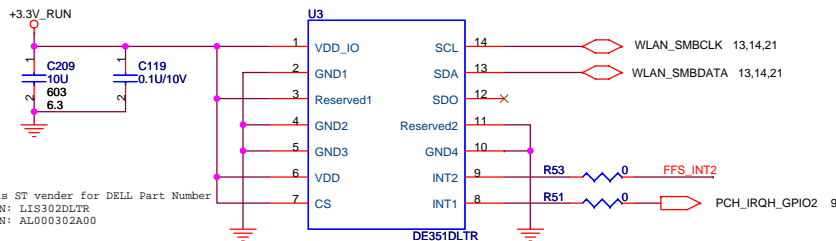
SATA Connector.



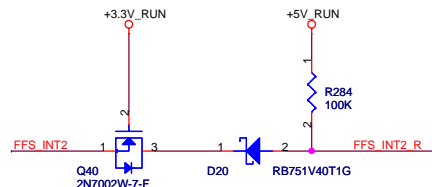
ODD Connector

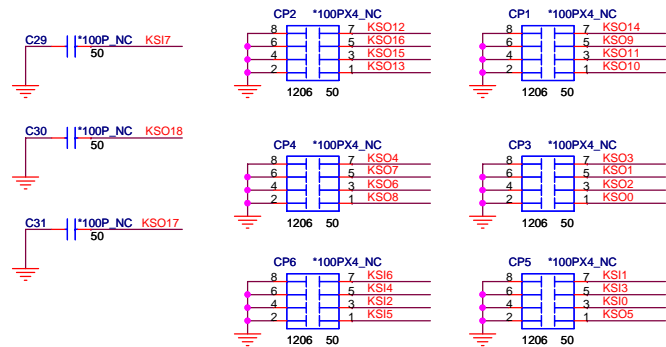
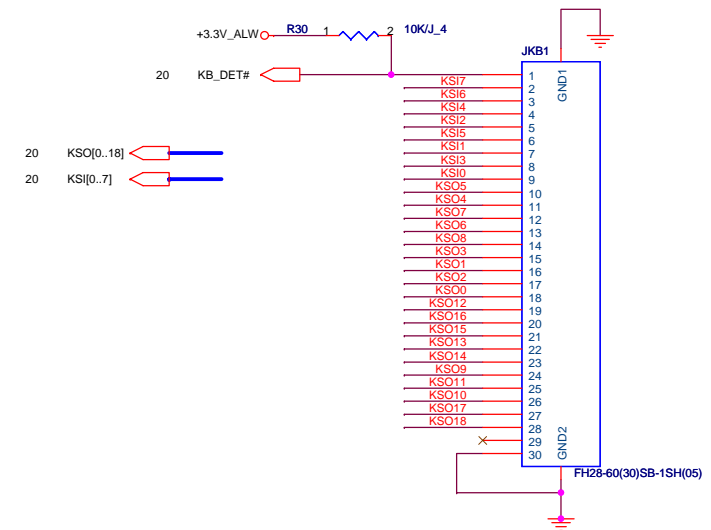
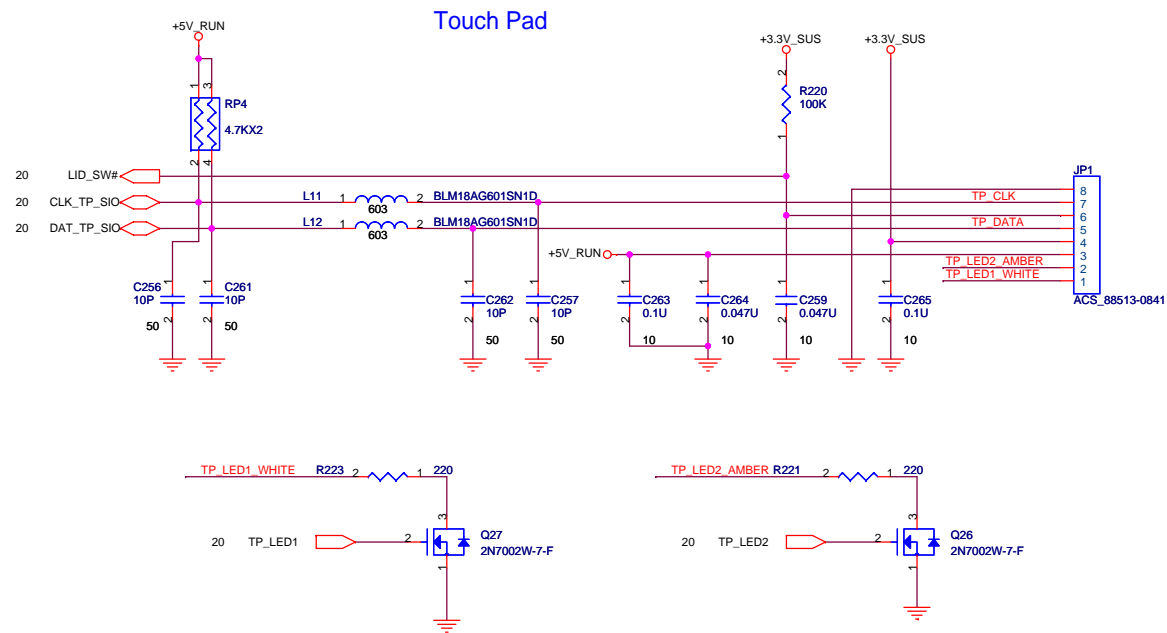


3-axis Fall Sensor (HDD data protector)



DE351DL is ST vender for DELL Part Number
Vender PN: L15302DLTR
Quanta PN: AL000302A00

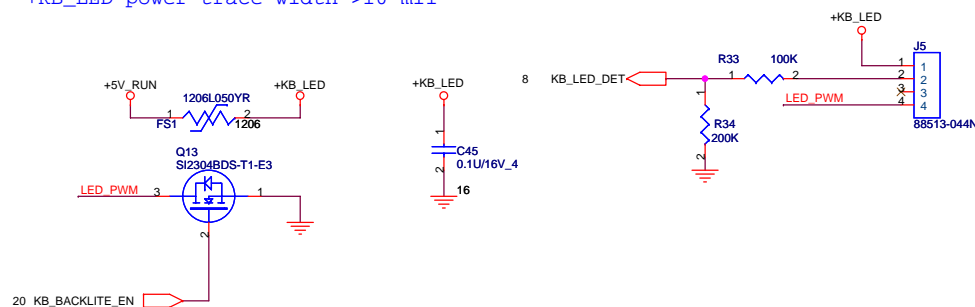




100P CAPS CLOSE TO JKB1

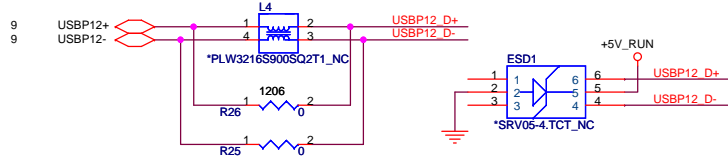
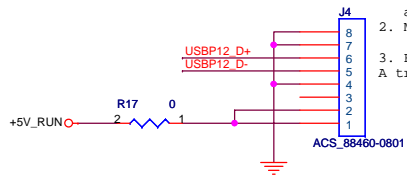
Key board illumination

```
+KB_LED power trace width >10 mil
```

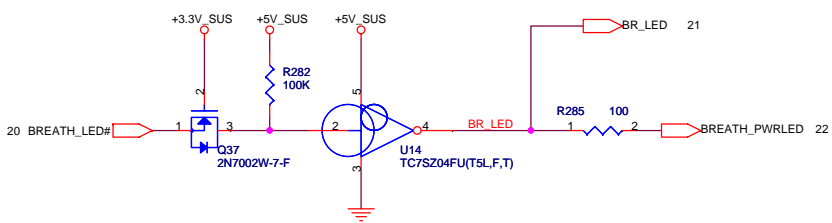
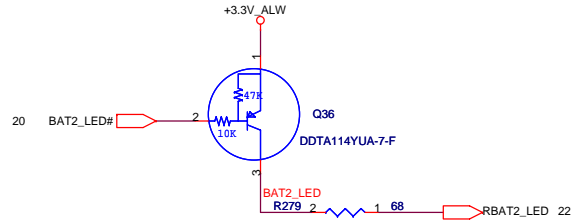
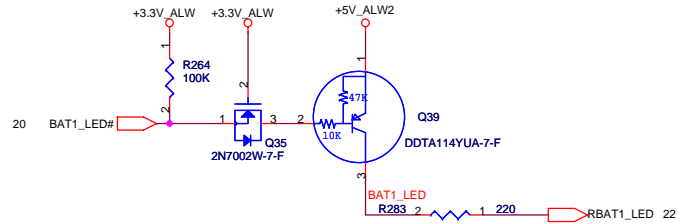


Touch Screen Module

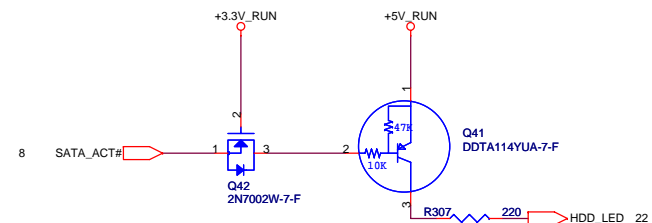
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



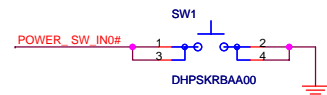
Battery status.



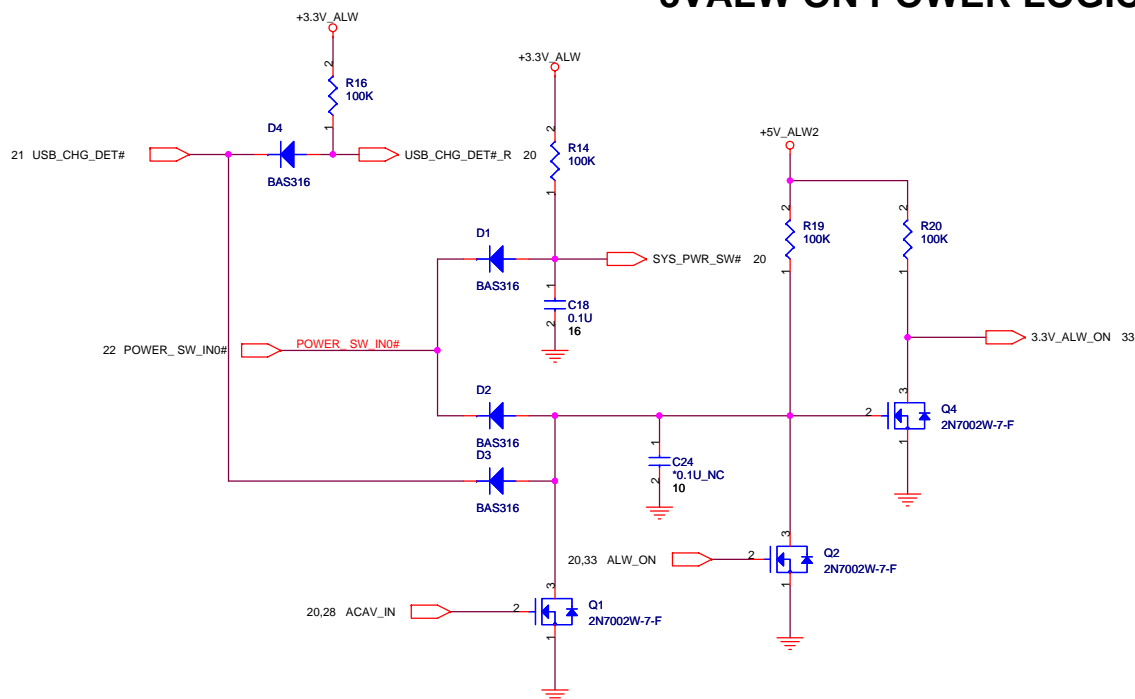
HDD activity LED.



Power button for Engineer



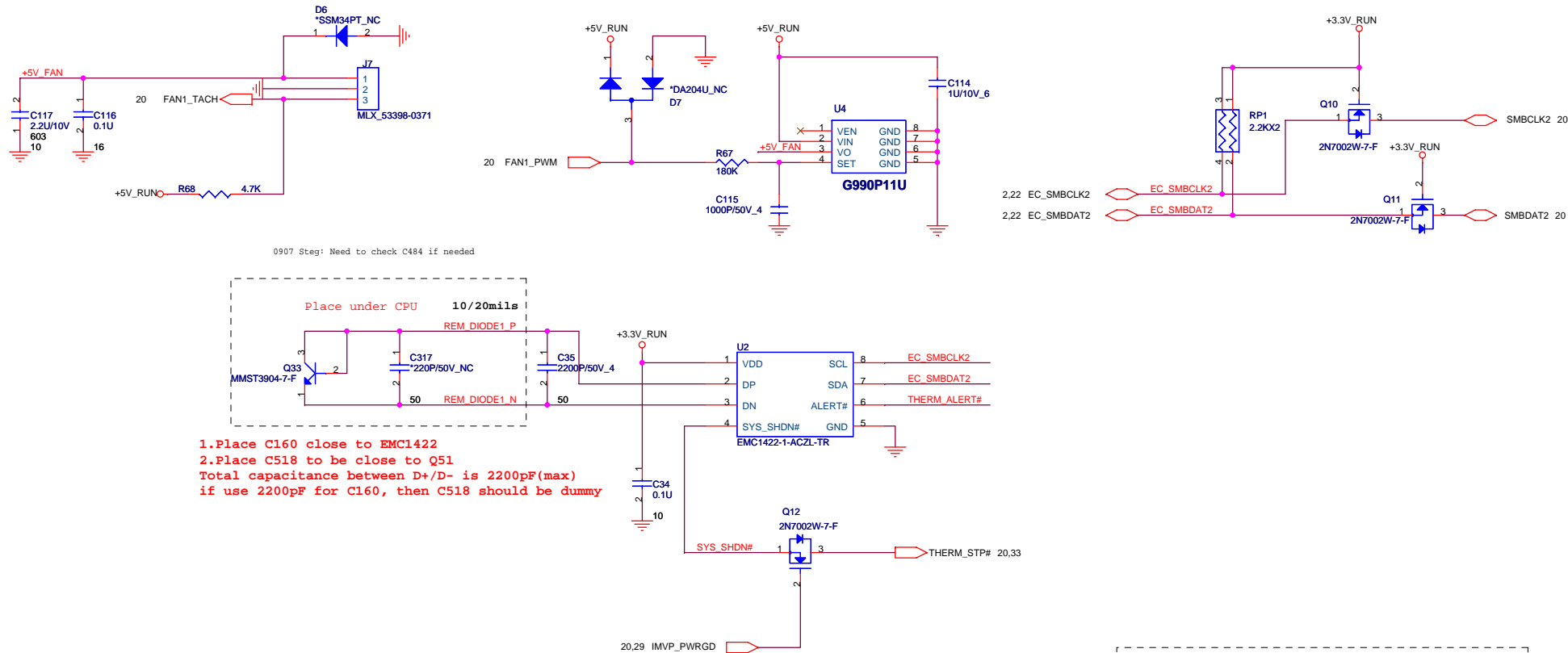
3VALW ON POWER LOGIC

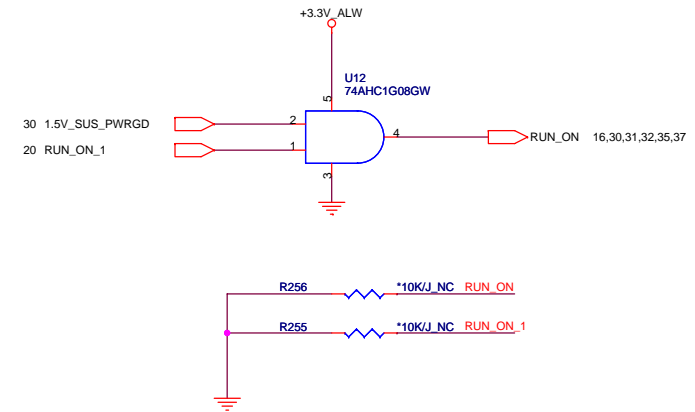
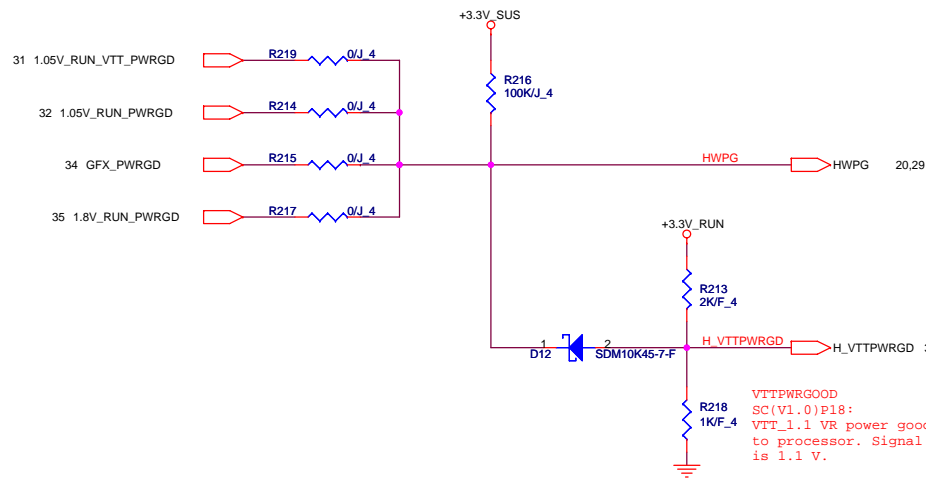
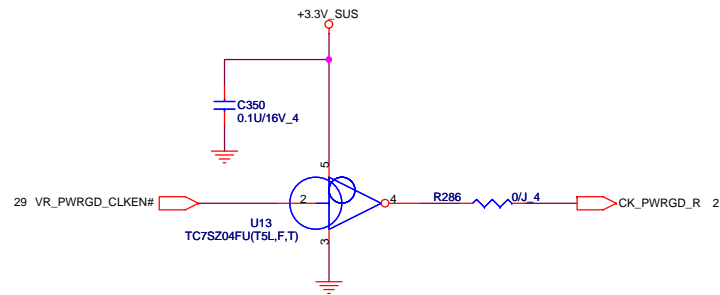


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PROJECT : Calpella UMA

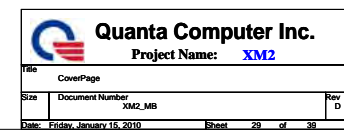
Size	Document Number	Rev
1A	SWITCH / LED / T-Screen	1A

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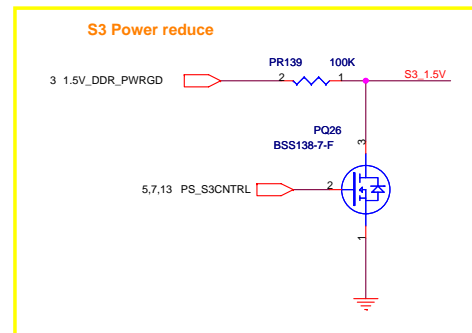








TON	PR67 = 620K
FREQ	400K



VFB = 0.75V

VDDQ and VTT discharge control

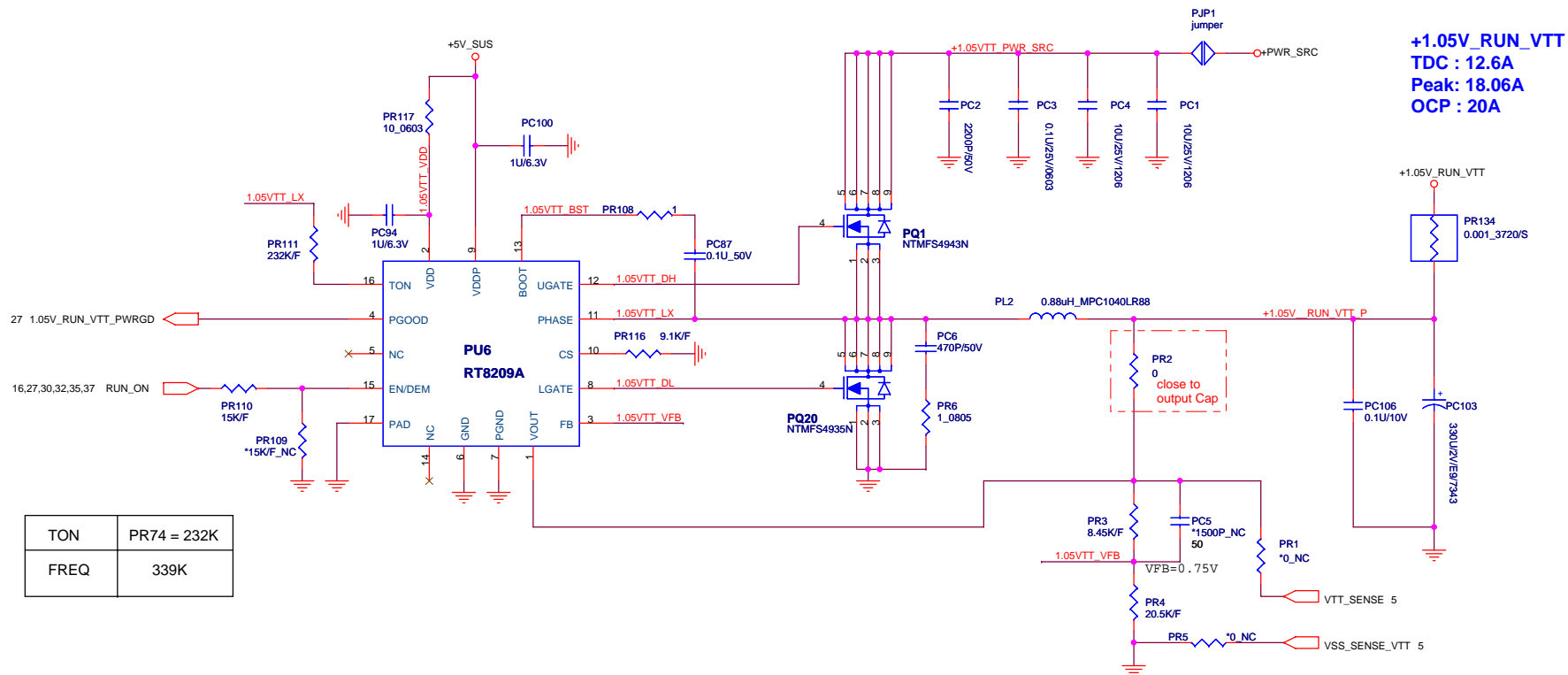
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

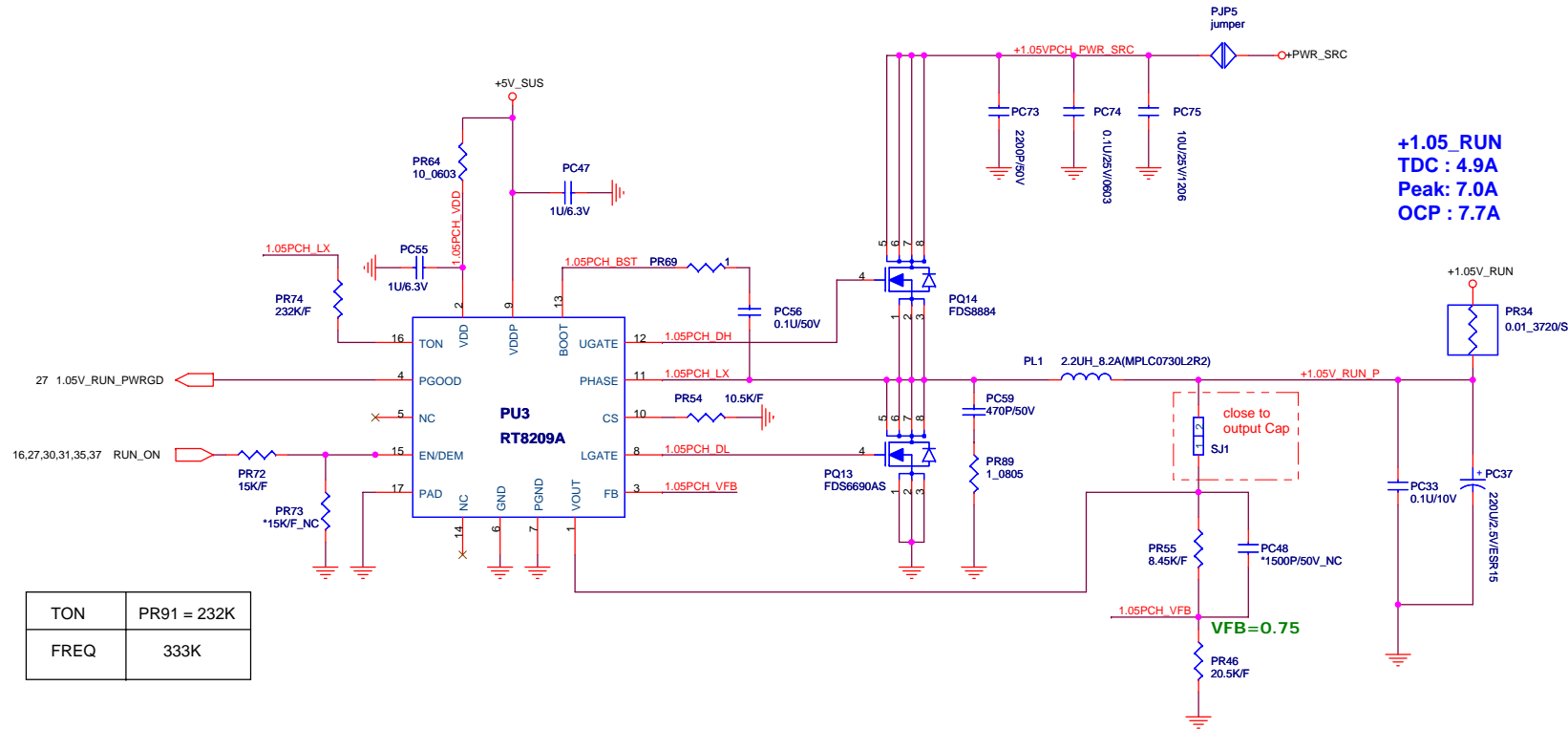
VDDQ output voltage selection

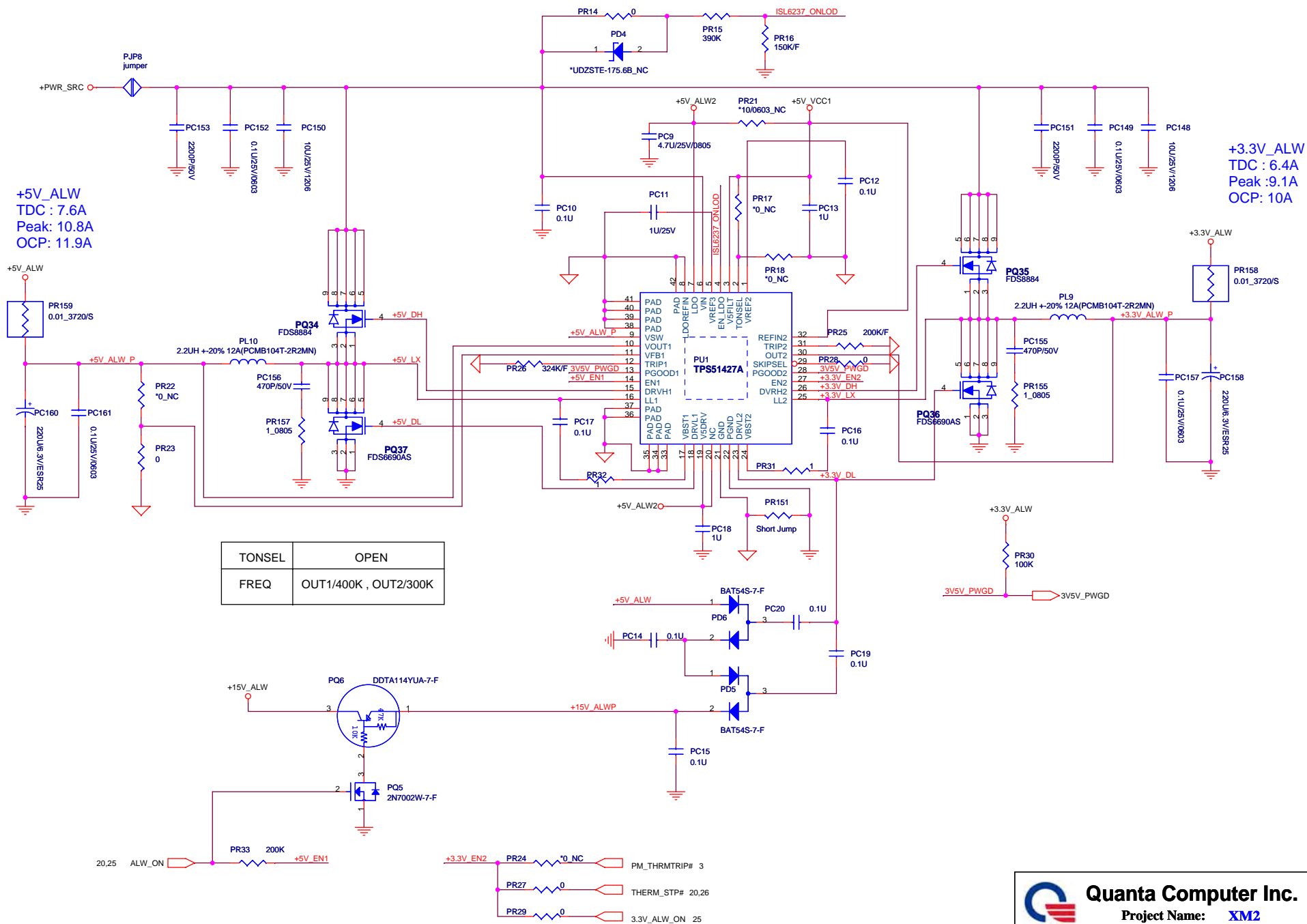
FB	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	$0.75V < VDDQ < 3.3V$

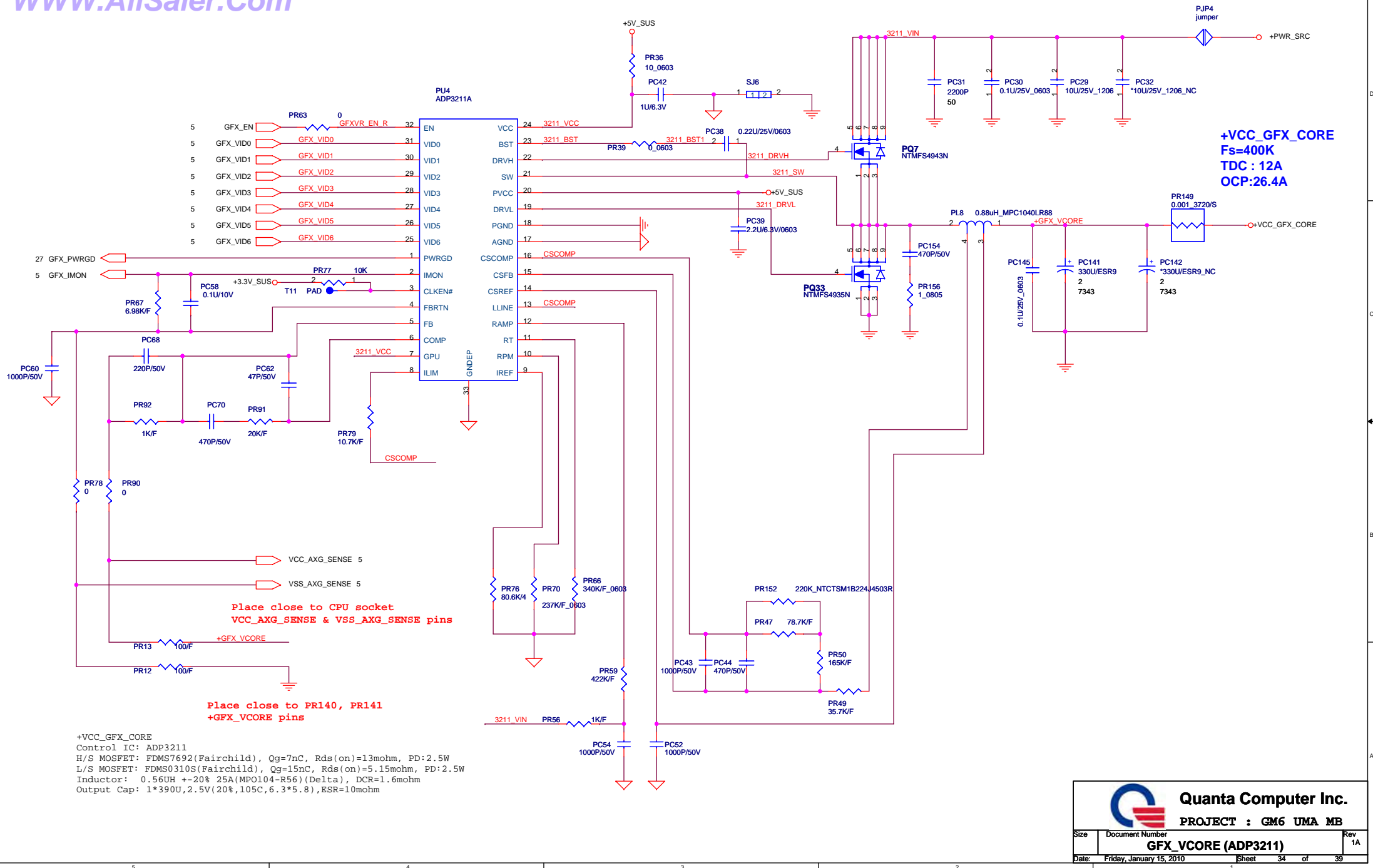
Outputs Management by S3, S5 control

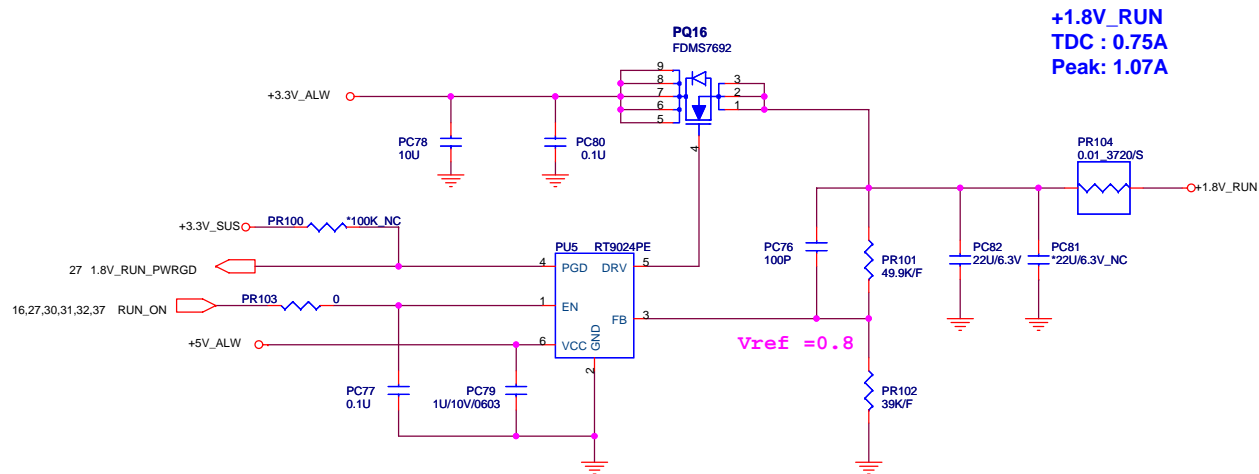
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

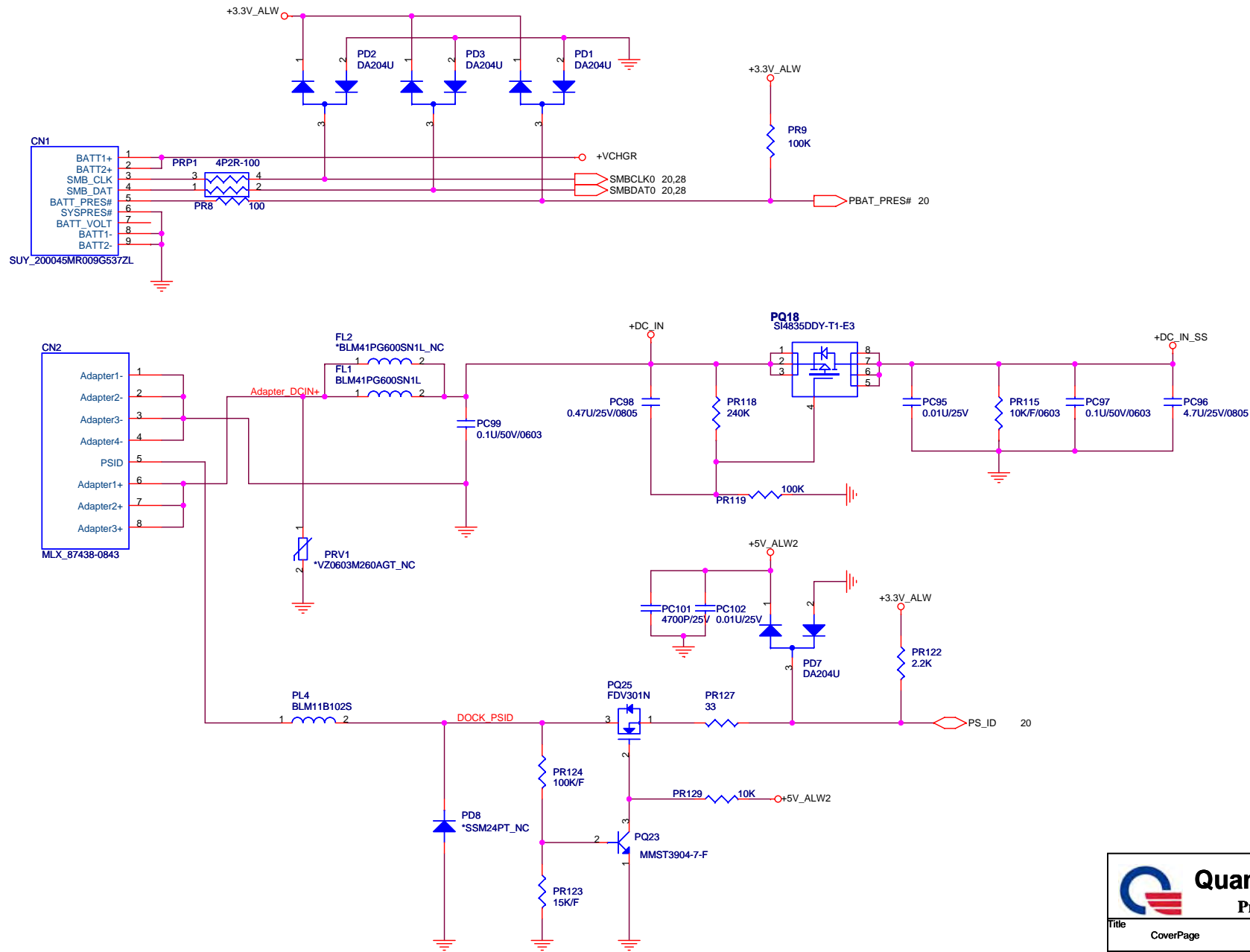


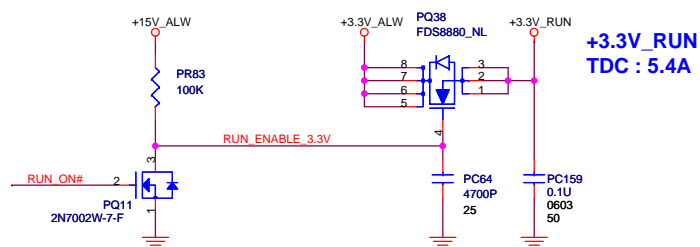
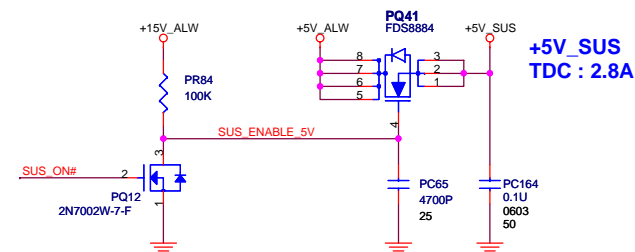
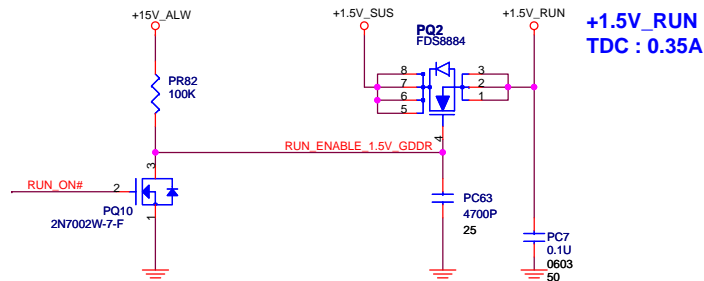
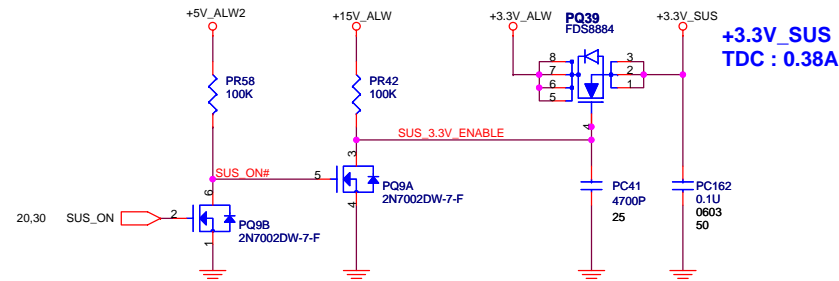
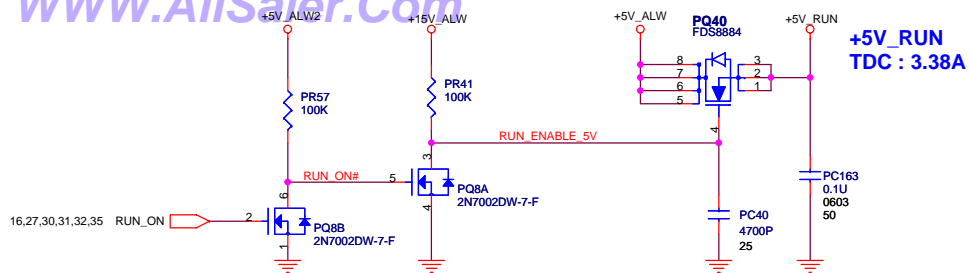




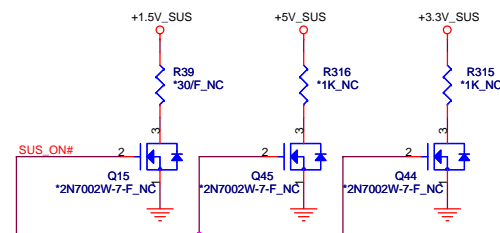
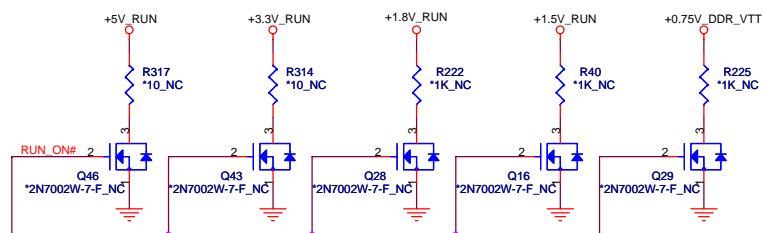





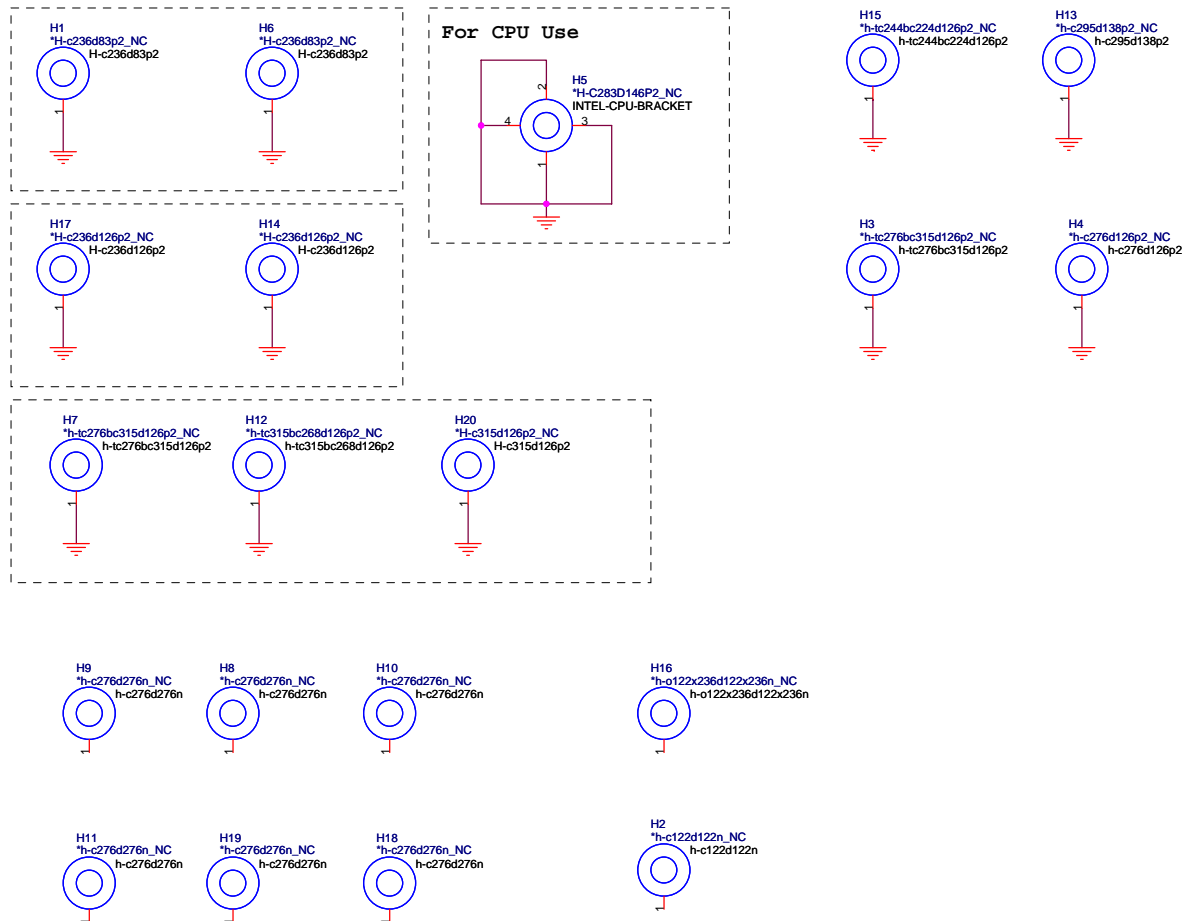





Reserve discharge path



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 Quanta Computer Inc. Project Name: GM7	
Title: PAD & SCREW	
Size: Document Number	Rev: D
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